

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Constantin Bulucea and Rebecca Rossen

Assignee:

Siliconix incorporated

Title:

Trench DMOS Power Transistor With Field-Shaping Body Proffle and

Three-Dimensional Geometry

Application No.:

08/851,608

Filed:

5 May 1997

Examiner:

S. Crane

Group Art Unit:

2811

Docket No.:

M-799-4C US

San Jose, California 23 December 2002

BOX CPA COMMISSIONER FOR PATENTS Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97(b)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, the documents listed on the accompanying substitute PTO Form 1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed, including translations where indicated. Copies of English abstracts of all the cited Japanese Patent Publications ("JPPs") are also enclosed, except for JPP 63-124762, a utility model JPP.

The present application is a file-wrapper continuation of parent U.S. patent application 08/453,285 which, in turn, is a file-wrapper continuation of grandparent U.S patent application 08/086,976. Hence all documents cited in parent application 08/453,285 and in grandparent application 08/086,976 are of record in the present application.

JPP 62-12167 was previously cited in grandparent application 08/086,976 and is re-cited here because an English translation of JPP 62-12167 is enclosed.

JPP 62-37965 was previously cited in grandparent application 08/086,976 using the partial number "0037965". JPP 62-37965 is re-cited here for clarity using its full publication

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25 METRO DRIVE, SUITE 700 SAN JOSE, CA 95110 (408) 453-9200 FAX (408) 453-7979 number. Also, the JPP 62-37965 publication date, previously given as 15 February 1987, is corrected here to 18 February 1987.

Blanchard, "Optimization of High Power MOS Transistors", was cited in parent application 08/453,285 and is re-cited here to identify the page numbers and indicate that the document is a Ph.D. dissertation.

Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET -- Static Shield V-MOSFET", was cited earlier in this application and is re-cited here because a copy of the Japanese version of the document is enclosed.

Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", was cited earlier in this application using the partial title "U-MOS Power FET" and is re-cited here (a) to present the full title and (b) because an English translation is enclosed. Inasmuch as the Japanese version of Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", has two sets of page numbers, both sets of page numbers "335 - 442" and "143 - 150" are included here in the citation rather than the single set of page numbers "143 - 150" previously used in the citation.

Applicants' attorney does not have an English translation of Kato et al, "A Study for High Voltage V-MOS Structure". However, Kato et al, "A Study for High Voltage V-MOS Structure", appears to deal with material similar to that in Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET", and similar to that in Katoh et al, "Design of High Breakdown V-MOSFET Applying Static Shield Effect".

Applicants' attorney recognizes that the enclosed copies of some of the cited documents repeat copies previously provided to the PTO in connection with the present application, with parent application 08/453,285, or with grandparent application 08/086,976. To the extent that such accumulation of multiple copies may be inconsistent with PTO policy or rules, Applicants' attorney requests the Examiner to discard the earlier-provided copies.

Further enclosed to simplify printing of the present application is a Summary of all the Documents Cited, i.e., now of record, in the present application and suitable for being listed on the first page of the patent as "References Cited". In the enclosed Summary of Cited Documents, the citations for some of the journal articles have been simplified by deleting unnecessary material such as the names of authors after the first-named authors.

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Siliconix inc. ("Siliconix"), the assignee of the present application, is also the assignee of (a) U.S. Patent 5,072,266, the great grandparent of the present application, and (b) U.S. Patent 5,298,442, the great grandparent of the present application.

Siliconix sued Fairchild Semiconductor Corp. ("Fairchild") for infringement of U.S. Patents 5,072,266 and 5,298,442. The patent infringement suit, now settled, was brought in the Northern District of California as case no. 99-04797 SBA. In the infringement suit, Fairchild submitted a 66-page Response Chart in which Fairchild alleged that certain claims of U.S. Patents 5,072,266 and 5,298,442 were invalid as anticipated by, or/and obvious in view of, certain references cited in the Response Chart.

A copy of the Response Chart, dated 30 August 2000, is enclosed. Subject to the comments in the next two paragraphs, all of the documents cited in the Response Chart are included with the enclosed substitute PTO Form 1449 or are already of record in the present application including parent application 08/753,285 and grandparent application 08/086,976. Likewise, aside from the documents already of record in the present application, copies of all the documents cited in the Response Chart are included with the enclosed copies of the references cited in the substitute PTO Form 1449.

On page 3 of the Response Chart, the citation to Kato et al, "A Study of High Voltage V-MOS Structure", should apparently be Kato et al, "A Study for High Voltage V-MOS Structure". That is, "of" in the title should apparently be "for".

Page 3 of the Response Chart cites (a) Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect," IEICE Transactions C, Vol. 66, No. 6, 1983, and then (b) Kato et al, "High Voltage-ization Using Static Shield Effect", Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984. As far as applicants' attorney can determine, these two documents are respective English and Japanese versions of a single reference. Also, the journal/date citation information appears to be wrong for the English version, item (a). Referring to the enclosed substitute PTO Form 1449 and the accompanying copies of the cited documents, items (a) and (b) appear to be Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect", Review of the Electrical Communications Laboratories (which is probably an alternative English translation of the Japanese journal translated into English as Electrical Communications

Laboratories Technical Journal for item b) while the remaining citation information is Vol.

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FAX (408) 453-7979

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32, No. 6, 1984, pages 1107-1114, for the English version, and Vol. 33, No. 2, 1984, pages 257-268, for the Japanese version.

In the Siliconix/Fairchild patent infringement suit, Fairchild also submitted an Amended Initial Disclosure of Defendant Fairchild Semiconductor – Prior Art in which Fairchild cited over five hundred references, including references cited in the Response Chart.

A copy of this Amended Initial Prior Art Disclosure, likewise dated 30 August 2000, is enclosed.

Certain of the references cited in the Amended Initial Prior Art Disclosure are classified as "102" or/and "103" references with respect to U.S. Patents 5,072,266 and 5,298,442. However, the Amended Initial Prior Art Disclosure does not cite any particular claim(s) of U.S. Patents 5,072,266 and 5,298,442, and does not provide any analogies between any of the claims of U.S. Patents 5,072,266 and 5,298,442, on one hand, and the material of any of the cited references, including the "102", "102/103", and "103" references, on the other hand. All of the "102" references, including three "102" references not mentioned in the Response Chart, are listed on the accompanying substitute PTO Form 1449 or are already of record in the present application.

Aside from the references cited in both the enclosed substitute PTO Form 1449 and the Amended Initial Prior Art Disclosure, Applicants' attorney has not obtained copies of and/or reviewed any of the further references cited in the Amended Initial Prior Art Disclosure in connection with the present application, and expresses no view as to the materiality of any of these further references to any of the claims of this application. The enclosed copy of the Amended Initial Prior Art Disclosure is provided in fulfillment of applicants' attorneys' obligation of candor and good faith with the PTO.

If the Response Chart and the Amended Initial Prior Art Disclosure themselves need to be listed on a (substitute) PTO Form 1449 in order for the Examiner to be obligated to consider these two Fairchild documents, please so inform Applicants' attorney.

Citation of the above documents shall not be construed as:

- 1. an admission that the documents are necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made; or

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5 METRO DRIVE, SUITE 700 SAN JOSE, CA 95110 (408) 453-9200 FAX (408) 453-7979 3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Please telephone Applicants' attorney at 408-453-9200, ext. 1371, if there are any questions regarding this submission.

EXPRESS MAIL LABEL NO.

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Respectfully submitted,

Ronald J. Meetin

Attorney for Applicants

Reg. No. 29,089

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TERRENCE P. McMAHON (State Bar No. 71910) WILLIAM L. ANTHONY, JR. (State Bar No. 106908)

MONTE COOPER (State Bar No. 196746)

KAI TSENG (State Bar No. 193756)

THOMAS J. GRAY (State Bar No. 191411)

ORRICK, HERRINGTON & SUTCLIFFE LLP

1020 Marsh Road

Menlo Park, CA 94025

Telephone: (650) 614-7400

Facsimile: (650) 614-7401

Attorneys for Defendant

FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

(OAKLAND DIVISION)

SILICONIX INCORPORATED, a Delaware corporation,

Plaintiff.

CASE NO. 99-04797 SBA

RESPONSE CHART (Civil L.R. 16-9(b))

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FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,

Defendant.

Pursuant to Civil Local Rule 16-9(b), Fairchild Semiconductor Corporation ("Fairchild") herein serves its response chart on Plaintiff Siliconix Incorporated Siliconix"). Fairchild provides the following claim invalidity analysis under 35 U.S.C. §§ 102 and 103.

INTRODUCTION I.

Local Rule 16-9(a) requires that the party alleging infringement of a patent must submit a claim chart which "must contain" information identifying "where each element of each infringed claim is found within each apparatus, product [or] device . . .". L.R. 16-9(a)(4). Siliconix's claim chart alleges that Claim 1 of U.S. Patent No. 5,072,266 ("the '266 patent") and Claims 17, 18, 19, 20, 22, 23 and 24 of U.S. Patent No. 5,298,442 ("the '442 patent") are infringed by the Fairchild FDS 6680A product. Siliconix has failed to provide a claim chart which applies the asserted claims of the '266 patent and '442 patent against any other Fairchild product. DOCSSV2:500277.1

ORRICK HERRINGTON & SUTCLIFFE LLP RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

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Accordingly, Siliconix should be precluded from asserting infringement of the '266 patent and/or '422 patent against any other Fairchild product.

II. RESPONSIVE CHART

The following chart indicates which claims of the patent are anticipated by which pieces of prior art. Please note that the information in this document is provisional and subject to revision, for the following reasons:

- (i) Fairchild's position on the invalidity of particular claims will depend on how those claims are construed by the Court. Because claim construction has not yet occurred, Fairchild cannot take a final position on the bases for invalidity of disputed claims because the Court may construe those claims to mean something different from what Fairchild presently assumes them to mean.
 - (ii) Fairchild has not yet completed its search for prior art.
- (iii) Fairchild has not completed its discovery from Plaintiff. Depositions of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventor, for instance, will likely reveal information that affects the conclusions herein.

Fairchild reserves the right to revise and/or supplement the claim chart. Fairchild incorporates herein the prosecution file history of the '266 patent and the '442 patent.

Presently, Fairchild intends to rely upon the following prior art patents and references:

JP 55146976

JP 58137254

JP 62-16572 -

Physics and Technology of Power MOSFETs, Shi-Chung Sun, UMI Dissertation Services,

February 1982

Optimization of Discrete High Power MOS Transistors, Richard A. Blanchard, UMI

Dissertation Services, Dec. 1981

JP 62012167

U.S. Patent 4,420,379

DOCSSV2:500277.1

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1	JP 63-124762
2	JP 63-224260
3	JP 59-181668
4	JP 54-57871
5	JP 57-72365
6	JP 59-193064
7	JP 60-28271
8	JP_57-18365
9	JP 59-80970
10	U.S. Patent 4,345,265
11	U.S. Patent 4,443,931
12	U.S. Patent 4,532,534
13	U.S. Patent 4,374,455
14	U.S. Patent 4,767,722
15	U.S. Patent 3,412,297
16	U.S. Patent 4,783,694
17	U.S. Patent 4,593,302
18	Design of New Structural High Breakdown Voltage V-MOSFET – Static Shield V-
19	MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in
20	. Japan, Vol. 66-C, No. 6, 1983
21	A Study of High Voltage V-MOS Structure, Kunihara Kato, et al., IEICE Transactions C.,
22	Vol. 81, No. 7(ED81-4), 1981.
23	Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara
24	Kato, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.
25	High Voltage-ization Using Static Shield Effect, Kunihara Kato, et al., Electrical
26	Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.
27	U-MOS Power MOSFET, Daisuke Ueda, et al., National Technical Report, Vol. 29, No. 2,
28	Apr. 1983

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DOCSSV2:500277.1

RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

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The Following References (referred hereinafter as "KATOH") W	Vill Be Analyzed Together:
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Design of New Structural High Breakdown Voltage V-MOSFET – Static Shield V-

MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in Japan, Vol. 66-C, No. 6, 1983

A Study of High Voltage V-MOS Structure, Kunihara Katoh, et al., IEICE Transactions C., Vol. 81, No. 7(ED81-4), 1981.

Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara Katoh, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.

High Voltage-ization Using Static Shield Effect, Kunihara Katoh, et al., Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.

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13	INVALIDITY CLAIM CHART FO	R U.S. PATENT NO. 5,072,266
14	U.S. Patent 5,072,266	JP 55146976
14	CLAIM 1	
15	1. A trench DMOS transistor cell comprising:	Double Diffusion Insulating Gate Field Effect Transistor
1.5	a substrate of semiconductor material of heavily doped	N+ layer (101)
16	first electrical conductivity type;	
- •	a first covering layer of semiconductor material of said	N- layer (102)
17	first electrical conductivity type lying on the substrate;	
	a second covering layer of semiconductor material of	P layer (3)
18	second electrical conductivity type lying on the first	
	covering layer;	77.1 (10.0)
19	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (104)
	having a top surface and partly lying over the second	the P layer (3) has a heavily doped P+ region (103)
20	covering layer, wherein a portion of the second covering	which extends upward through the N+ layer (104) and
٠.	layer is heavily doped and this portion extends both	which extends downward (110-1 and 110-2) into the N-
21	vertically upward and downward, an upward portion	layer (102)
22	extending through the third covering layer to the top	
22	surface of the third covering layer and a downward	
23	portion extending downward into the first covering	·
	layer;	
24	a trench having a bottom surface and side surfaces and	trench (5) with a bottom surface and side surfaces which
	extending vertically downward from the top surface of	extend vertically downward from the top surface of the
25	the third covering layer through the third covering layer	N+ layer (104) through the N+ layer (104), the P layer
	and the second covering layer and through a portion of	(3) and through a portion of the N- (102) layer, wherein the bottom surface of the trench (5) lies above a lowest
26	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	part of the downward portion of the P+ region of the P
_	portion of the second covering layer;	layer.
27	electrically conducting semiconductor material	semiconductor material (107)
20	positioned within the trench;	semiconductor material (107)
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	a layer of oxide positioned within the trench between the	oxide (106)
	electrically conducting semiconductor material and the	
:	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
,	conducting semiconductor material, to the third covering	material (107), to the N+ layer (104) and to the N+
	layer and to the substrate, respectively.	substrate (101).

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6	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442		
7	U.S. Patent No. 5,298,442	JP 55146976	
7	CLAIM 17		
8	17. A method for providing a transistor, said method	Double Diffusion Insulating Gate Field Effect Transisto	
	comprising the steps of:	Nt laver (101) and N. laver (102)	
9	providing a first region of a first conductivity type;	N+ layer (101) and N- layer (102)	
0	providing a second region of a second conductivity type over said first region;	P layer (3) formed by a first diffusion	
U	providing a third region of said first conductivity type	N+ layer (104) formed by a second diffusion	
1	such that said first and third regions are separated by said second region;		
,	providing a trench through said third and second	trench (5) with a bottom surface and side surfaces whic	
2	regions; and	extend vertically downward from the top surface of the	
3	, .	N+ layer (104) through the N+ layer (104), the P layer	
כ		(3) and through a portion of the N- (102) layer.	
4	providing a gate in said trench;	Al gate electrode (107)	
•	wherein a portion P of said second region, which portion	the P layer (3) has a heavily doped P+ region (103)	
5	is spaced from said trench, extends deeper than said	which extends upward through the N+ layer (104) and	
,	trench so that, if a predetermined voltage is applied to	which extends downward (110-1 and 110-2) through the	
,	said gate and to said third region and another	N- layer (102) deeper than the trench (5)	
,	predetermined voltage is applied to said first region, an		
,	avalanche breakdown occurs away from a surface of		
	said trench.		
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,	CLAIM 18		
	18. The method of claim 17 wherein said portion P of	the P layer (3) has a heavily doped P+ region (103)	
)	said second region is doped heavier than another portion	laterally spaced from the trench (5)	
	of said second region which portion is adjacent said	·	
	trench.		
	CLAIM 19		
	19. The method of claim 17 wherein said first region	N+ layer (101) under N- layer (102)	
	comprises a first portion and a second portion over said	·	
	first portion, said second portion being lighter doped		
	than said first portion.		
	CLAIM 20		
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown	
	breakdown is a reach-through breakdown across said	across the N- layer (102)	
	second portion.		
'	CLAIM 22	·	
7	21. The method of claim 17 further comprising the step	oxide (106)	
'	of providing an insulator between said surface of said		
3	trench and said gate.		
,		DECROSION ON A DE DIMESTA A METO COME I D. 14 A	

1	CLAIM 23	
2	23. A method for providing a transistor, said method comprising the steps of:	Double Diffusion Insulating Gate Field Effect Transistor
3	providing a first region of a first conductivity type; providing a second region of said first conductivity type	N+ layer (101)
_	over said first region, said second region being lighter	N- layer (102)
4	doped than said first region;	71 (2) 6
5	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3) formed by a first diffusion
6	providing a fourth region of said first conductivity type over said third region;	N+ layer (104) formed by a second diffusion
. 7	providing a trench through said fourth region and third	trench (5) with a bottom surface and side surfaces which
8	regions; and	extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer (3) and through a portion of the N- (102) layer.
9	providing a gate in said trench;	Al gate electrode (107)
10	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (3) is laterally spaced from said trench
11	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (3) and the N+ layer (101) is less than a depletion width of a
12	width of a planar junction which has the same doping profile as does said junction between said second and	planar junction which has the same doping profile as does the junction between the N- layer (102) and the P
13	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
14	CLAIM 24	
15	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the deepest part of the P layer (3) is heavier doped (P+ region(103)) than the part of the P layer (3) adjacent trench (5)
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U.S. Patent 5,072,266	JP 58137254
CLAIM 1	
A trench DMOS transistor cell comprising:	Insulated Gate Semiconductor Device See Fig. 7
ubstrate of semiconductor material of heavily doped st electrical conductivity type;	N+ layer (1)
first covering layer of semiconductor material of said rest electrical conductivity type lying on the substrate;	N- layer (2)
econd covering layer of semiconductor material of ond electrical conductivity type lying on the first ering layer;	P layer (13)

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1	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (14);
2	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	the P layer (13) has a heavily doped P+ region (19) portion which extends upward through the N+ layer (14)
3	layer is heavily doped and this portion extends both	and which extends downward into the N- layer (2)
4	vertically upward and downward, an upward portion extending through the third covering layer to the top	
4	surface of the third covering layer and a downward	
5	portion extending downward into the first covering	
	layer;	
6	a trench having a bottom surface and side surfaces and	trench with a bottom surface and side surfaces which
	extending vertically downward from the top surface of	extend vertically downward from the top surface of the
7	the third covering layer through the third covering layer	N+ layer (14) through the N+ layer (104), the P layer
	and the second covering layer and through a portion of	(13) and through a portion of the N- (19) layer, wherein
8	the first covering layer, wherein the bottom surface of	the bottom surface of the trench lies above a lowest part
	the trench lies above a lowest part of the downward	of the downward portion of the P+ region of the P layer.
9	portion of the second covering layer;	
i	electrically conducting semiconductor material	gate semiconductor material (17)
10	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide insulating film (16)
11	electrically conducting semiconductor material and the	
ļ	bottom and side surfaces of the trench; and	
12	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the gate
	conducting semiconductor material, to the third covering	semiconductor material (17), to the N+ layer (14) and to
13	layer and to the substrate, respectively.	the N+ substrate (1).
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U.S. Patent No. 5,298,442	JP 58137254
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Insulated Gate Semiconductor Device See Fig. 7
providing a first region of a first conductivity type;	N+ layer (1) and N- layer (2)
providing a second region of a second conductivity type over said first region;	P layer (13) formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (14) formed by a second diffusion
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (14) through the N+ layer (14), the P layer (1
	and through a portion of the N- (2) layer.
providing a gate in said trench;	gate semiconductor material (17)

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1	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the P layer (13) has a heavily doped P+ region (19) which extends upward through the N+ layer (14) and
2	trench so that, if a predetermined voltage is applied to said gate and to said third region and another	which extends downward through the N- layer (2) deeper than the trench
3	predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
4	said trench.	•
5		·
	CLAIM 18	
6	18. The method of claim 17 wherein said portion P of	the P layer (13) has a heavily doped P+ region (19)
7	said second region is doped heavier than another portion of said second region which portion is adjacent said	which is laterally spaced from the trench
8	trench.	
	CLAIM 19	NT: 1(1) 4 NT 1(2)
, 9	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	N+ layer (1) under N- layer (2)
	first portion, said second portion being lighter doped	·
10	than said first portion.	
	CLAIM 20	
11	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
	breakdown is a reach-through breakdown across said	across the N- layer (2)
12	second portion.	1 101000 <u>10</u> 10 11.
12	CLAIM 22	•
13	21. The method of claim 17 further comprising the step	oxide insulating film (16)
14	of providing an insulator between said surface of said	onder districting min (10)
14	trench and said gate.	
15	CLAIM 23	
	23. A method for providing a transistor, said method	Insulated Gate Semiconductor Device
16	comprising the steps of:	
	providing a first region of a first conductivity type;	N+ layer (1)
17	providing a second region of said first conductivity type	N- Layer (2)
	over said first region, said second region being lighter	
18	doped than said first region;	
	providing a third region of a second conductivity type	P layer (13) formed by a first diffusion
19	over said second region, said second and third regions	
	forming a junction;	
20	providing a fourth region of said first conductivity type over said third region;	N+ layer (14) formed by a second diffusion
21	providing a trench through said fourth region and third	V trench which extends vertically downward from the
22	regions; and	top surface of the N+ layer (14) through the N+ layer
22		(14), the P layer (13) and through a portion of the N- (2)
23		layer.
23	providing a gate in said trench;	gate electrode (17)
24	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (13) is laterally spaced from said V trench
25	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (13)
د2	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a
26	width of a planar junction which has the same doping	planar junction which has the same doping profile as
20	profile as does said junction between said second and	does the junction between the N- layer (2) and the P layer
27	third regions at said deepest part of said third region and	(13) at the deepest part of the P layer (13) and which is
21	which is reverse biased around its breakdown voltage.	reverse biased around its breakdown voltage
	l	

1	CLAIM 24	
2	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (13) has a heavily doped P+ region (19) which is laterally spaced from the trench
3		

	U.S. Patent 5,072,266	
5	CLAIM 1	JP 6216572
	1. A trench DMOS transistor cell comprising:	Vertical-type Semiconductor Device and Manufacturing Method Therefore
	,	See figs. 1(a) and 1(b)
	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate:	N layer (2)
	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	N+ layer (8) (p. 11 of translation: "Contracted by an n+, type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short portions underneath the n+-type semiconductor layer 8.")
•	vertically upward and downward, an upward portion extending through the third covering layer to the top	p. 11 of translation: "Forming p+-type semiconductor layers 3 in cells by photolithography is used as another
1	surface of the third covering layer and a downward portion extending downward into the first covering layer;	way of reducing the likelihood of the punch-through phenomenon occurring in conventional DSA MOS FETs."
		the P layer (4) has a heavily doped P+ region (3) portion which extends upward through the N+ layer (1) and which extends downward into the N layer (2)
•	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is
	the third covering layer through the third covering layer and the second covering layer and through a portion of	characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is
•	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	provided with a groove; a semiconductor film or conductor film pattern formed through the agency of a first inculating film are the semiconductor film or conductor film pattern formed through the agency of a
	portion of the second covering layer;	first insulating film over the groove formed in the principal surface of the semiconductor substrate"
	·	As seen from Fig. 1(b), the P layer (4) has a heavily
		doped P+ region (3) portion which extends upward through the N+ layer (8) and which extends downward into the N layer (2)
	electrically conducting semiconductor material positioned within the trench;	source Al electrode 9 is formed on this insulating film
	·	p. 12 of translation: " a semiconductor film or conductor film pattern formed through the agency of a
	·	first insulating film over the groove formed in the
-	DOCSSV2:500277.1	principal surface of the semiconductor substrate"

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RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

1	a lover of oxide positioned within the tourt by	
1	a layer of oxide positioned within the trench between the	first insulating film (5a)
	electrically conducting semiconductor material and the	, ,
2	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	Source Al electrode (9a).
3	conducting semiconductor material, to the third covering	()
	layer and to the substrate, respectively.	Gate Al electrode (9b).
4		
		Since the device is a vertical-type semiconductor device,
5		the N+ layer (1) must have a drain electrode.

INVALIDITY CLAIM CHART FO U.S. Patent No. 5,298,442	JP 62-16572
CLAIM 17	
17. A method for providing a transistor, said method	Vertical-type Semiconductor Device and Manufacturi
comprising the steps of:	Method Therefore
	See figs. 1(a) and 1(b)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (4) with a P+ region (3).
providing a third region of said first conductivity type	N. 1 (0) (11 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
such that said first and third regions are separated by	N+ layer (8) (p. 11 of translation: "Contracted by an n
said second region;	type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short
said socolid region,	portions underneath the n+-type semiconductor layer 8
providing a trench through said third and second	p. 12 of translation: "The vertical-type semiconductor
regions; and	device in accordance with the present invention is
	characterized by comprising a semiconductor substrate
	a first conduction type whose principal surface is
	provided with a groove: "
providing a gate in said trench;	p. 12 of translation: "a semiconductor film or
•	conductor film pattern formed through the agency of a
	first insulating film over the groove formed in the
wherein a madis D of 11 1 1 1 1 1 1	principal surface of the semiconductor substrate"
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the P layer (4) has a heavily doped P+ region (3) whic
trench so that, if a predetermined voltage is applied to	extends upward through the N+ layer (8) and which
said gate and to said third region and another	extends downward through the N- layer (2) deeper that the groove
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CI AIM 10	
CLAIM 18	1 71
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	the P layer (4) has a heavily doped P+ region (3) which
of said second region which portion is adjacent said	spaced away from the groove
rench.	,
CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2).
comprises a first portion and a second portion over said	in layer (1) under in layer (2).
first portion, said second portion being lighter doped	
han said first portion.	

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1	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N layer (2)
	second portion.	
3	CLAIM 22	
	21. The method of claim 17 further comprising the step	first insulating film (5a)
4	of providing an insulator between said surface of said	\ , ,
	trench and said gate.	
5	CLAIM 23	
	23. A method for providing a transistor, said method	Vertical-type Semiconductor Device and Manufacturing
6	comprising the steps of:	Method Therefore
	tomprising are steps on	
. 7		See figs. 1(a) and 1(b)
	providing a first region of a first conductivity type;	N+ layer (1)
8	providing a second region of said first conductivity type	N layer (2)
	over said first region, said second region being lighter	1. 20,01 (2)
9	doped than said first region;	
	providing a third region of a second conductivity type	P layer (4)
10	over said second region, said second and third regions	1 16301 (T)
	forming a junction;	
11	providing a fourth region of said first conductivity type	N+ layer (8) (p. 11 of translation: "Contracted by an n+-
	over said third region;	type semiconductor layer 8, the p-type semiconductor
12	over said unite region,	layer 4 (channel region) thus forms long and short
		portions underneath the n+-type semiconductor layer 8.")
13		portions understand in a sypt commenced in the con-
	providing a trench through said fourth region and third	p. 12 of translation: "The vertical-type semiconductor
14	regions; and	device in accordance with the present invention is
	,,	characterized by comprising a semiconductor substrate of
15		a first conduction type whose principal surface is
	·	provided with a groove; a semiconductor film or
16		conductor film pattern formed through the agency of a
		first insulating film over the groove formed in the
17		principal surface of the semiconductor substrate"
18		As seen from Fig. 1(b), the P layer (4) has a heavily
		doped P+ region (3) portion which extends upward
19		through the N+ layer (8) and which extends downward
		into the N layer (2) p. 12 of translation: "The vertical-type semiconductor
20	providing a gate in said trench;	device in accordance with the present invention is
		characterized by comprising a semiconductor substrate of
21	·	a first conduction type whose principal surface is
		provided with a groove;"
22		
	,	p. 12 of translation: " a semiconductor film or
23		conductor film pattern formed through the agency of a
_		first insulating film over the groove formed in the
24		principal surface of the semiconductor substrate"
	wherein a deepest part of said third regions is laterally	P layer (4) is laterally spaced from said groove.
25	spaced from said trench;	

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wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer (4) at the deepest part of the P layer (4) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (4) has a heavily doped P+ region (3) which is spaced away from the groove

U.S. Patent 5,072,266	Physics and Technology of Power MOSFETs
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VDMOS – see Figs. 2.1, 2.21 and 3.21
a substrate of semiconductor material of heavily doped	N+ layer
first electrical conductivity type;	
a first covering layer of semiconductor material of said	N- layer
first electrical conductivity type lying on the substrate;	
a second covering layer of semiconductor material of	P layer
second electrical conductivity type lying on the first	
covering layer;	
a third covering layer of semiconductor material of	N+ layer
heavily doped said first electrical conductivity type and	1
having a top surface and partly lying over the second	As seen in Fig. 2.1, a portion of the P layer is neavily
covering layer, wherein a portion of the second coveri	doped P+; the P+ region extends vertically upward
layer is heavily doped and this portion extends both	around the N+ layer and downward into the N- layer
vertically upward and downward, an upward portion	
extending through the third covering layer to the top	
surface of the third covering layer and a downward	
portion extending downward into the first covering	
layer;	
a trench having a bottom surface and side surfaces and	trench with a bottom surface and side surfaces which
extending vertically downward from the top surface of	extend vertically downward from the top surface of the
the third covering layer through the third covering layer	N+ layer through the N+ layer, the P layer and through
and the second covering layer and through a portion o	portion of the N- layer.
the first covering layer, wherein the bottom surface of	
the trench lies above a lowest part of the downward	
portion of the second covering layer;	
electrically conducting semiconductor material	semiconductor material
positioned within the trench;	
a layer of oxide positioned within the trench between	the oxide between the trench and gate
electrically conducting semiconductor material and th	e
bottom and side surfaces of the trench; and	
three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semicondu
conducting semiconductor material, to the third cover	material, to the top N+ layer and to the N+ substrate.
layer and to the substrate, respectively.	

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	U.S. Patent No. 5,298,442	Physics and Technology of Power MOSFETs
_	CLAIM 17	
	7. A method for providing a transistor, said method comprising the steps of:	VDMOS – see Figs. 2.1, 2.21 and 3.21
	providing a first region of a first conductivity type;	N+ layer substrate and N- layer
p	providing a second region of a second conductivity type over said first region;	P layer formed by a first diffusion
p s	providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer formed by a second diffusion
F	providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through portion of the N- layer.
-	providing a gate in said trench;	Al gate electrode
Ī	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the P layer has a heavily doped P+ region which extend upward through the N+ layer and which extends
t	rench so that, if a predetermined voltage is applied to said gate and to said third region and another	downward through the N- layer deeper than the trench.
ľ	predetermined voltage is applied to said first region, an	
a	avalanche breakdown occurs away from a surface of said trench.	
┢	CLAIM 18	
1	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
41	trench.	
L	CLAIM 19	N+ layer substrate under the N- layer
	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	11. Myor oncomment and a 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.
1	first portion, said second portion being lighter doped	
L	than said first portion. CLAIM 20	
١	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	avalanche breakdown is a reach-through breakdown across the N- layer
L	second portion. CLAIM 22	
	21. The method of claim 17 further comprising the step of providing an insulator between said surface of said	oxide between the trench and gate
	trench and said gate. CLAIM 23	
	23. A method for providing a transistor, said method comprising the steps of:	VDMOS – see Figs. 2.1, 2.21 and 3.21
	providing a first region of a first conductivity type;	N+ layer
	providing a second region of said first conductivity type	N- Layer

1 2	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer formed by a first diffusion
3	providing a fourth region of said first conductivity type over said third region;	N+ layer formed by a second diffusion
4	providing a trench through said fourth region and third regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
Ì	providing a gate in said trench;	Al gate electrode
6	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer is laterally spaced from said trench
7	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer and the N+ layer is less than a depletion width of a planar
8	width of a planar junction which has the same doping profile as does said junction between said second and	junction which has the same doping profile as does the junction between the N- layer and the P layer at the
9	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	deepest part of the P layer and which is reverse biased around its breakdown voltage
10	CLAIM 24	mount in ordered in the second
11	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
12	mile region which put is adjacent serie acree.	1

U.S. Patent 5,072,266	Optimization of Discrete High Power MOS Transistors
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS Structure – see Fig. 4.22
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer;
having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	the P layer has a heavily doped P+ region portion which extends upward through the N+ layer and which extend
layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	downward into the N layer.
extending through the third covering layer to the top surface of the third covering layer and a downward	
portion extending downward into the first covering layer:	
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the
the third covering layer through the third covering layer and the second covering layer and through a portion of	N+ layer through the N+ layer, the P layer and through portion of the N- layer.

1.

1	the first covering layer, wherein the bottom surface of	
	the trench lies above a lowest part of the downward	
2	portion of the second covering layer;	
-	electrically conducting semiconductor material	semiconductor material
3	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide between the trench and gate
4	electrically conducting semiconductor material and the	
	bottom and side surfaces of the trench; and	
5	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
	conducting semiconductor material, to the third covering	material, to the top N+ layer and to the N+ substrate.
6	layer and to the substrate, respectively.	

` [U.S. Patent No. 5,298,442	Optimization of Discrete High Power MOS Transistors
) -	CLAIM 17	
	7. A method for providing a transistor, said method omprising the steps of:	VMOS Structure – see Fig. 4.22
2 P	providing a first region of a first conductivity type;	N+ layer substrate and N- layer
p	providing a second region of a second conductivity type over said first region;	P layer formed by a first diffusion
p	providing a third region of said first conductivity type	N+ layer formed by a second diffusion
s	uch that said first and third regions are separated by aid second region;	
r	providing a trench through said third and second egions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through
5		portion of the N- layer.
. [providing a gate in said trench;	Al gate electrode
v	wherein a portion P of said second region, which portion s spaced from said trench, extends deeper than said rench so that, if a predetermined voltage is applied to	the P layer has a heavily doped P+ region which extend upward through the N+ layer and which extends downward through the N- layer deeper than the trench.
s	said gate and to said third region and another oredetermined voltage is applied to said first region, an	
a	avalanche breakdown occurs away from a surface of said trench.	· ·
	•	,
: ├	CLAIM 18	
} s	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
	of said second region which portion is adjacent said trench.	
5	CLAIM 19	N. 1
- 11	19. The method of claim 17 wherein said first region	N+ layer substrate under the N- layer
5	comprises a first portion and a second portion over said	
	first portion, said second portion being lighter doped	

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1	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N- layer.
	second portion.	
3	CLAIM 22	
	21. The method of claim 17 further comprising the step	oxide between the trench and gate
4	of providing an insulator between said surface of said	
	trench and said gate.	
5	CLAIM 23	
_	23. A method for providing a transistor, said method	VMOS Structure – see Fig. 4.22
6	comprising the steps of:	
_	providing a first region of a first conductivity type;	N+ layer
7	providing a second region of said first conductivity type	N- Layer
	over said first region, said second region being lighter	·
8	doped than said first region;	
	providing a third region of a second conductivity type	P layer formed by a first diffusion
9	over said second region, said second and third regions	
10	forming a junction;	
10	providing a fourth region of said first conductivity type	N+ layer formed by a second diffusion
11	over said third region;	
. **	providing a trench through said fourth region and third	trench with a bottom surface and side surfaces which
12	regions; and	extend vertically downward from the top surface of the
		N+ layer through the N+ layer, the P layer and through a
13		portion of the N- layer.
	providing a gate in said trench;	Al gate electrode
14	wherein a deepest part of said third regions is laterally	P layer is laterally spaced from said trench
	spaced from said trench;	
15	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer and
	third region and said first region is less than a depletion	the N+ layer is less than a depletion width of a planar
16	width of a planar junction which has the same doping	junction which has the same doping profile as does the
	profile as does said junction between said second and	junction between the N- layer and the P layer at the
17	third regions at said deepest part of said third region and	deepest part of the P layer and which is reverse biased around its breakdown voltage
	which is reverse biased around its breakdown voltage. CLAIM 24	around its breakdown voltage
18		the P layer has a heavily doped P+ region which is
	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said	laterally spaced away from the trench
19	third region which part is adjacent said trench.	l laterary spaced away from the deficit
	unid region which part is adjacent said denon.	

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	U.S. Patent 5,072,266	JP 62012167
3 [CLAIM 1	
4	1. A trench DMOS transistor cell comprising:	Manufacture of Vertical Type Semiconductor Device with Groove Section
5		See fig. 1(f).
6	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (11) (p. 5 of the translation: "a n+-type semiconductor substrate 11 with a high concentration of impurities is coated with an n-type semiconductor layer
7 L		12 having a lower concentration of impurities.")
- :	a first covering layer of semiconductor material of said	N layer (12)
8	first electrical conductivity type lying on the substrate;	
	DOCSSV2:500277.1	RESPONSE CHART PURSUANT TO CIVIL L.R. 16-90

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RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

1	a second covering layer of semiconductor material of	P layer (16)
	second electrical conductivity type lying on the first	
2	covering layer;	
	a third covering layer of semiconductor material of	N+ layer (17) lying partly over the P layer (16)
3	heavily doped said first electrical conductivity type and	
	having a top surface and partly lying over the second	P layer (16) extends vertically upward through the N+
4	covering layer, wherein a portion of the second covering	layer (17) to the top surface and downward into the N
	layer is heavily doped and this portion extends both	layer (12)
5	vertically upward and downward, an upward portion	
	extending through the third covering layer to the top	
6	surface of the third covering layer and a downward	,
	portion extending downward into the first covering	
7	layer;	
•	a trench having a bottom surface and side surfaces and	p. 6 of translation: "The grooved portion 20 has smooth
8	extending vertically downward from the top surface of	outlines and does not have any sharp pointed sections."
-	the third covering layer through the third covering layer	
9	and the second covering layer and through a portion of	As seen from fig. 1(f), the grooved portion (20) extends
	the first covering layer, wherein the bottom surface of	upward through the N+ layer (17) and which extends
10	the trench lies above a lowest part of the downward	downward into the P layer (16) and the N layer (12)
- 0	portion of the second covering layer;	
11	electrically conducting semiconductor material	p. 6 of translation: " polycrystalline silicon film 22
	positioned within the trench;	constituting a gate electrode"
12	a layer of oxide positioned within the trench between the	gate oxide film (21)
	electrically conducting semiconductor material and the	,
13	bottom and side surfaces of the trench; and	•
	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
14	conducting semiconductor material, to the third covering	material (22), to the top N+ layer (17) and to the N+
• •	layer and to the substrate, respectively.	substrate (11).
15	layer and to the substrate, respectively.	
	li .	•

U.S. Patent No. 5,298,442	JP 62012167
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Manufacture of Vertical Type Semiconductor Device with Groove Section
	See fig. 1(f).
providing a first region of a first conductivity type;	N+ layer (11) and N layer (12).
providing a second region-of a second conductivity type over said first region;	P layer (16).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (17) lying above the P layer (16).
providing a trench through said third and second regions; and	p. 6 of translation: "The grooved portion 20 has smooth outlines and does not have any sharp pointed sections."
	As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
providing a gate in said trench;	gate oxide film (21)

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1 2 3	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	the P layer (16) extends upward through the N+ layer (17) and which extends downward through the N layer (12) deeper than the grooved portion (20)
4	said trench.	
5		
6	CLAIM 18	
Ŭ	18. The method of claim 17 wherein said portion P of	N/A
7	said second region is doped heavier than another portion	
	of said second region which portion is adjacent said	
8	trench.	•
	CLAIM 19	
9	19. The method of claim 17 wherein said first region	N+ substrate (11) under N layer (12)
	comprises a first portion and a second portion over said	
0	first portion, said second portion being lighter doped	•
	than said first portion. CLAIM 20	
1		
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said second portion.	across the N layer (12)
	CLAIM 22	
3		-
	21. The method of claim 17 further comprising the step	gate oxide (21)
4	of providing an insulator between said surface of said trench and said gate.	
_	CLAIM 23	
5		
6	23. A method for providing a transistor, said method comprising the steps of:	Manufacture of Vertical Type Semiconductor Device
0	comprising the steps of:	with Groove Section
7	· ·	Son #= 1/0
′	providing a first region of a first conductivity town	See fig. 1(f).
8	providing a first region of a first conductivity type; providing a second region of said first conductivity type	N+ layer (11)
o .	over said first region, said second region being lighter	N layer (12)
9	doped than said first region;	
	providing a third region of a second conductivity type	P layer (16)
0	over said second region, said second and third regions	1 layer (10)
	forming a junction;	
1	providing a fourth region of said first conductivity type	N+ layer (17) lying above the P layer (16)
	over said third region;	14 layer (17) lying above the F layer (10)
2	providing a trench through said fourth region and third	p. 6 of translation: "The grooved portion 20 has smooth
	regions; and	outlines and does not have any sharp pointed sections."
3	rogions, and	outlines and does not have any snarp pointed sections.
4		As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends
ا ۔		downward into the P layer (16) and the N layer (12)
5	providing a gate in said trench; wherein a deepest part of said third regions is laterally	gate oxide film (21)
	triparam a doomast most of said third series is let seller	P layer (16) is laterally spaced from said groove.

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-19-

wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (16) and the N+ layer (11) is less than a depletion width of a
width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	planar junction which has the same doping profile as does the junction between the N- layer (12) and the P layer (16) at the deepest part of the P layer (16) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	N/A

7	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
8	- U.S. Patent 5,072,266	U.S. Patent 4,420,379
	CLAIM 1	, , , , , , , , , , , , , , , , , , , ,
9	1. A trench DMOS transistor cell comprising:	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Self-
10		Aligned, Non Planar, MOS Transistor
11		See Figs. 3-19.
12	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (20)
13	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N- layer (21)
14	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (22), (25) and (27)
15	a third covering layer of semiconductor material of	N+ layer (26)
16	heavily doped said first electrical conductivity type and having a top surface and partly lying over the second	the P layer has a heavily doped P+ region (22) which
17	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	extends upward through the N+ layer (26) and which extends downward into the N- layer (21)
18	vertically upward and downward, an upward portion extending through the third covering layer to the top	Col. 4, lns. 23-26: "In the stage shown as FIG. 5, the device undergoes an oxidizing treatment which
19	surface of the third covering layer and a downward portion extending downward into the first covering	simultaneously deepens the P+ type guard ring and protects the peripheral part of the junction under a thick
20	layer;	oxide layer 23 (1 micron), called the field oxide."
21	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench (30) with a bottom surface and side surfaces which extend vertically downward from the top surface of the
22	the third covering layer through the third covering layer and the second covering layer and through a portion of	N+ layer (26) through the N+ layer (26), the P layer (25) and through a portion of the N- (21) layer, wherein the bottom surface of the trench (30) lies above a lowest part
23	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	of the downward portion of the P layer (22)
24	portion of the second covering layer; electrically conducting semiconductor material positioned within the trench;	semiconductor material (32)
25	a layer of oxide positioned within the trench between the	oxide (31)
26	electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	
27	three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	gate semiconductor material (32), source electrode (33) and drain at N+ substrate (20)
28	layer and to the substrate, respectively.	

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U.S. Patent No. 5,298,442	U.S. Patent No. 4,420,379
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Se Aligned, Non Planar, MOS Transistor
	See Figs. 3-19.
providing a first region of a first conductivity type;	N+ layer (20) and N- layer (21)
providing a second region of a second conductivity type over said first region;	P layer (22), (25) and (27)
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (26)
providing a trench through said third and second regions; and	trench (30) through the N+ layer (26), the P layer (25) and through a portion of the N- (21) layer
providing a gate in said trench;	gate semiconductor material (32)
wherein a portion P of said second region, which portion	a portion of the P layer (22), which portion is spaced
is spaced from said trench, extends deeper than said	from the trench (30), extends deeper than the trench (3
trench so that, if a predetermined voltage is applied to	· ·
said gate and to said third region and another	a portion of the P Layer (22) acts as a guard rail to spre
predetermined voltage is applied to said first region, an	the electric field at the periphery and away from the
avalanche breakdown occurs away from a surface of said trench.	channel.
CLAIM 18	
18. The method of claim 17 wherein said portion P of	P layer has a heavily doped P+ portion (22) which is
said second region is doped heavier than another portion of said second region which portion is adjacent said trench.	laterally spaced from the trench
CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (20) under N- layer (21)
comprises a first portion and a second portion over said	11. Tayor (20) under 11- tayer (21)
first portion, said second portion being lighter doped	
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
oreakdown is a reach-through breakdown across said second portion.	across the N- layer (21)
CLAIM 22	
21. The method of claim 17 further comprising the step	oxide (31)
of providing an insulator between said surface of said rench and said gate.	
CLAIM 23	
23. A method for providing a transistor, said method	Method for the Formation of Polycrystalline Silicon
comprising the steps of:	Layers, and its Application in the Manufacture of a Self Aligned, Non Planar, MOS Transistor
	See Figs. 3-19.
	N+ layer (20)

1	providing a second region of said first conductivity type over said first region, said second region being lighter	N- layer (21)
2	doped than said first region;	T (20) (25) 1 (25)
3	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (22), (25) and (27)
4	providing a fourth region of said first conductivity type over said third region;	N+ layer (26)
5	providing a trench through said fourth region and third regions; and	trench (30) through the N+ layer (26) and the P layer (25) and through a portion of the N- (21) layer
6	providing a gate in said trench;	gate semiconductor material (32)
7	wherein a deepest part of said third regions is laterally spaced from said trench;	the P layer region (22) is laterally spaced from trench (30)
8	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (22) and the N+ layer (20) is less than a depletion width of a
9	width of a planar junction which has the same doping profile as does said junction between said second and	planar junction which has the same doping profile as does the junction between the N- layer (21) and the P
10	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	layer (22) at the deepest part of the P layer (22) and which is reverse biased around its breakdown voltage
11	CLAIM 24	
11	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ and is doped
12	said third region is doped heavier than a part of said third region which part is adjacent said trench.	heavier than the part of the third region P (25) adjacent the trench
Ī	1	

U.S. Patent 5,072,266	JP 63-124762
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Vertical MOSFET
	See fig. 1
a substrate of semiconductor material of heavily doped	N+ layer (1)
first electrical conductivity type;	
a first covering layer of semiconductor material of said	N layer (2)
first electrical conductivity type lying on the substrate;	
a second covering layer of semiconductor material of	P layer (3), (11) and (12)
second electrical conductivity type lying on the first	
covering layer;	
a third covering layer of semiconductor material of	N+ layer (4) lying partly over the P layer (3)
heavily doped said first electrical conductivity type and	
having a top surface and partly lying over the second	A portion of the P layer (11) and (12) is heavily doped
covering layer, wherein a portion of the second covering	P+ and extends upward through the N+ layer (4) to the
layer is heavily doped and this portion extends both	top and downward into the N layer (2).
vertically upward and downward, an upward portion	
extending through the third covering layer to the top	
surface of the third covering layer and a downward	·
portion extending downward into the first covering	
layer;	though (0) having a harron number and side and
a trench having a bottom surface and side surfaces and	trench (8) having a bottom surface and side surfaces an extending vertically downward from the top surface of
extending vertically downward from the top surface of	the N+ layer (4) through the N+ layer (4) and the P layer
the third covering layer through the third covering layer DOCSSV2:500277.1	RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9

1 2	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	(3) and through a portion of the N layer (2), wherein the bottom surface of the trench (8) lies above a lowest part of the P+ layer (12)
	portion of the second covering layer;	
3	electrically conducting semiconductor material	trench (8) possess a highly doped poly-silicon gate
	positioned within the trench;	electrode (9)
4	a layer of oxide positioned within the trench between the	gate oxide film (7)
•	electrically conducting semiconductor material and the	
5	bottom and side surfaces of the trench; and	
,	three electrodes electrically coupled to the electrically	gate electrode (9), source electrode (14) and drain
_	mice electiones electrically coupled to the electrically	
6	conducting semiconductor material, to the third covering	electrode (15)
	layer and to the substrate, respectively.	
	H	

U.S. Patent No. 5,298,442	JP 63-124762
CLAIM 17	
17. A method for providing a transistor, said method	Vertical MOSFET
comprising the steps of:	San Fa 1
C. C. A southering	See fig. 1 N+ layer (1) and N layer (2)
providing a first region of a first conductivity type;	P layer (3), (11) and (12)
providing a second region of a second conductivity type	F layer (3), (11) and (12)
over said first region;	N+ layer (4) such that P layer (3) is between the N layer
providing a third region of said first conductivity type	(2) and the N+ layer (4)
such that said first and third regions are separated by	(2) and no 11 injury (1)
said second region; providing a trench through said third and second	trench (8) extending through the N+ layer (4) and the P
regions; and	layer (3)
providing a gate in said trench;	trench (8) possess a highly doped poly-silicon gate
providing a gate in said deficit,	electrode (9)
wherein a portion P of said second region, which portion	portion P+ (12) is spaced from trench (8) and extends
is spaced from said trench, extends deeper than said	deeper than said trench (8) so that, if a predetermined
trench so that, if a predetermined voltage is applied to	voltage is applied to the gate (9) and to N+ layer (4) and
said gate and to said third region and another	another predetermined voltage is applied to the N+ layer (1), an avalanche breakdown occurs away from a surface
predetermined voltage is applied to said first region, an	of the trench (8).
avalanche breakdown occurs away from a surface of	of the trench (b).
said trench.	
,	
CLAIM 18	(4) 1(10) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
18. The method of claim 17 wherein said portion P of	A portion of the P layer (11) and (12) is heavily doped
said second region is doped heavier than another portion	P+
of said second region which portion is adjacent said	P layer (3) is adjacent the trench (8)
trench.	1 tayer (7) is adjacent the denon (6)
CLAIM 19	N+ layer (1) under N layer (2)
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)
comprises a first portion and a second portion over said	
first portion, said second portion being lighter doped	
than said first portion.	

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1	CLAIM 20	
Ī	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N layer (2)
	second portion.	
3	CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide film (7)
4	of providing an insulator between said surface of said	
	trench and said gate.	
5	CLAIM 23	
	23. A method for providing a transistor, said method	Vertical MOSFET
6	comprising the steps of:	
		See fig. 1
.7	providing a first region of a first conductivity type;	N+ layer (1)
	providing a second region of said first conductivity type	N layer (2)
8	over said first region, said second region being lighter	,
9	doped than said first region;	
9	providing a third region of a second conductivity type	P layer (3), (11) and (12) over N layer (2)
10	over said second region, said second and third regions	
. 10	forming a junction;	27.1 (2)
11	providing a fourth region of said first conductivity type	N+ layer (4) lying above the P layer (3).
* *	over said third region;	1 (0) (11 N) I I I I I I I I I I I I I I I I I I
12	providing a trench through said fourth region and third	trench (8) through N+ layer (4) and P layer (3)
	regions; and	:1- C1 (0)
13	providing a gate in said trench;	gate oxide film (9)
	wherein a deepest part of said third regions is laterally	portions of P layer (11) and (12) are laterally spaced from
14	spaced from said trench;	trench (8)
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (12)
15	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as
	width of a planar junction which has the same doping	does the junction between the N- layer (2) and the P layer
16	profile as does said junction between said second and	(12) at the deepest part of the P layer (12) and which is
	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	reverse biased around its breakdown voltage
17	CLAIM 24	1070130 Oldood drounds 110 Oldandown Youngs
	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ (12) and is
18	said third region is doped heavier than a part of said	doped heavier than the part of the third region P (3)
		adjacent the trench (8)
19	third region which part is adjacent said trench.	adjustit die denen (e)

VMOS FET
See fig. 1
P layer (11) (opposite conductivity type with respect to drain).
N- layer (12)
P layer (13) (20) lying on N layer (12)

11		
1	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (14) lying partly over the P layer (13), wherein a portion of the P layer (20) is heavily doped P+ and
2	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	extends downward into the N- Layer (12)
3	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	
4	extending through the third covering layer to the top surface of the third covering layer and a downward	
5	portion extending downward into the first covering layer;	
6	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench (15) having a bottom surface and side surfaces and extends vertically downward from the top surface of N+
7	the third covering layer through the third covering layer and the second covering layer and through a portion of	layer (14) through the N+ layer (14) and the P layer (13) and through a portion of the N- layer (12), wherein the bottom surface of the trench (15) lies above the lowest
8	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	part of the downward portion of the P layer (20) which is heavily doped
9	portion of the second covering layer; electrically conducting semiconductor material positioned within the trench;	poly gate material (18) in trench (15)
10	a layer of oxide positioned within the trench between the	gate oxide film (17)
11	electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	
12	three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	gate electrode (18), source electrode (9) and drain electrode (24)
13	layer and to the substrate, respectively.	

U.S. Patent No. 5,298,442	JP 63-224260
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of :	See fig. 1
providing a first region of a first conductivity type;	N- layer (12).
providing a second region of a second conductivity type over said first region;	P layer (16) and (20)
providing a third region of said first conductivity type	N+ layer (14) lying above the P layer (16)
such that said first and third regions are separated by said second region;	
providing a trench through said third and second regions; and	trench (15) extends through N+ layer (17) and P layer (16)
providing a gate in said trench;	poly gate (18)
wherein a portion P of said second region, which portion	a portion of the P layer (20) is laterally spaced from the
is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	trench (15) and extends deeper than the trench (15)
said gate and to said third region and another predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of said trench.	

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1	CLAIM 18	
	18. The method of claim 17 wherein said portion P of	a portion P of the P layer is P+ (20) and is doped heavier
2	said second region is doped heavier than another portion	than the portion (26) of the P layer adjacent the trench
	of said second region which portion is adjacent said	(15)
3	trench.	
ľ	CLAIM 19	
4	19. The method of claim 17 wherein said first region	N/A
Ì	comprises a first portion and a second portion over said	
5	first portion, said second portion being lighter doped	•
	than said first portion.	
6	CLAIM 20	
Ì	20. The method of claim 19 wherein said avalanche	N/A
7	breakdown is a reach-through breakdown across said	
	second portion.	
8	CLAIM 22	
h	21. The method of claim 17 further comprising the step	gate oxide film (17)
9	of providing an insulator between said surface of said	
'	trench and said gate.	•
10	CLAIM 23	
	23. A method for providing a transistor, said method	VMOS FET
11	comprising the steps of:	, , , , , , , , , , , , , , , , , , , ,
	comprising the steps of	See fig. 1.
12	providing a first region of a first conductivity type;	P substrate (11)
l	providing a second region of said first conductivity type	N layer (12)
13	over said first region, said second region being lighter	- · · · · · · · · · · · · · · · · · · ·
	doped than said first region;	<u>.</u>
14	providing a third region of a second conductivity type	P layer (13) and (20)
	over said second region, said second and third regions	
15	forming a junction;	
.	providing a fourth region of said first conductivity type	N+ layer (14) lying above P layer (13)
16	over said third region;	
,,	providing a trench through said fourth region and third	trench (15) extending through N+ layer (13) and P layer
17	regions; and	(13)
18	providing a gate in said trench;	poly gate (18)
10	wherein a deepest part of said third regions is laterally	the deepest part of the P layer (20) is laterally spaced
19	spaced from said trench;	from trench (15)
19	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (20)
20	third region and said first region is less than a depletion	and the P layer (11) is less than a depletion width of a
20	width of a planar junction which has the same doping	planar junction which has the same doping profile as
21	profile as does said junction between said second and	does the junction between the N- layer (12) and the P
	third regions at said deepest part of said third region and	layer (20) at the deepest part of the P layer (20) and
22	which is reverse biased around its breakdown voltage.	which is reverse biased around its breakdown voltage
	CLAIM 24	
23	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ (20) which is
~-	said third region is doped heavier than a part of said	doped heavier than the part of the third region adjacent
24	third region which part is adjacent said trench.	the trench (15)

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U.S. Patent 5,072,266	JP 59-181668
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET
	See fig. 3
substrate of semiconductor material of heavily doped	N+ layer (11) and (12)
first electrical conductivity type;	, ()
a first covering layer of semiconductor material of said	N layer (13)
first electrical conductivity type lying on the substrate;	
a second covering layer of semiconductor material of	P layer (14) and (16) lying on N layer (13)
second electrical conductivity type lying on the first	
covering layer;	·
a third covering layer of semiconductor material of	N+ layer (15) lying partly over the P layer (14), wherein
heavily doped said first electrical conductivity type and	a portion of the P layer is a heavily doped P+ (16) and
having a top surface and partly lying over the second	extends vertically upward through the N+ layer (15) and
covering layer, wherein a portion of the second covering	vertically downward into the N layer (13)
ayer is heavily doped and this portion extends both	
vertically upward and downward, an upward portion	
extending through the third covering layer to the top	
surface of the third covering layer and a downward	
portion extending downward into the first covering ayer;	
a trench having a bottom surface and side surfaces and	trongle (21) having a harry and the Control of the
extending vertically downward from the top surface of	trench (21) having a bottom surface and side surface and extending vertically downward through the N+ layer
he third covering layer through the third covering layer	(15), the P layer (14) and through a portion of the N layer
and the second covering layer and through a portion of	(13), wherein the bottom surface of the trench (21) lies
he first covering layer, wherein the bottom surface of	above the lowest part of the P layer (16).
he trench lies above a lowest part of the downward	
portion of the second covering layer;	
electrically conducting semiconductor material	poly gate in trench (19)
positioned within the trench;	, , , , , , , , , , , , , , , , , ,
a layer of oxide positioned within the trench between the	gate oxide layer (17)
electrically conducting semiconductor material and the	
pottom and side surfaces of the trench; and	
hree electrodes electrically coupled to the electrically	gate electrode (19), source electrode (20) and drain
conducting semiconductor material, to the third covering	electrode (not shown)
ayer and to the substrate, respectively.	

23	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442		
43	U.S. Patent No. 5,298,442	JP 59-181668	
24	CLAIM 17		
25	17. A method for providing a transistor, said method comprising the steps of:	VMOS FET	
-5		See fig. 3	
26	providing a first region of a first conductivity type:	N+ layer (11) and (12), and N layer (13)	

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over said first region;

P layer (14) and (16) lying on N layer (13)

providing a second region of a second conductivity type

-		·
1	providing a third region of said first conductivity type such that said first and third regions are separated by	N+ layer (15) lying wherein N layer (13) and N+ layer (15) are separated by P layer (14)
2	said second region; providing a trench through said third and second	trench (21) extending vertically downward through the
3	regions; and	N+ layer (15) and P layer (14)
	providing a gate in said trench;	poly gate in trench (19)
4	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	a portion of the P layer (16), which is spaced from the trench, extends deeper than the trench (21)
6	said gate and to said third region and another predetermined voltage is applied to said first region, an	
7	avalanche breakdown occurs away from a surface of said trench.	
8		
9	CLAIM 18	
,	18. The method of claim 17 wherein said portion P of	a portion of the P layer (14) is a heavily doped P+ (16)
10	said second region is doped heavier than another portion of said second region which portion is adjacent said	which is laterally spaced from the trench (21)
11	trench. CLAIM 19	
12	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	N+ layer (11) and (12) under N layer (13)
13	first portion, said second portion being lighter doped than said first portion.	•
14	CLAIM 20	
15	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	avalanched breakdown is a reach-through breakdown across the N layer (13)
,,	second portion. CLAIM 22	
16	21. The method of claim 17 further comprising the step	gate oxide layer (17)
17	of providing an insulator between said surface of said trench and said gate.	
18	CLAIM 23	
19	23. A method for providing a transistor, said method comprising the steps of:	VMOS FET
20		See fig. 3
20	providing a first region of a first conductivity type; providing a second region of said first conductivity type	N+ layer (11) and (12) N layer (13)
21	over said first region, said second region being lighter doped than said first region;	N layer (13)
22	providing a third region of a second conductivity type	P layer (14) and (16) lying on N layer (13)
23	over said second region, said second and third regions forming a junction;	
24	providing a fourth region of said first conductivity type over said third region;	N+ layer (15) lying over the P layer (14)
25	providing a trench through said fourth region and third regions; and	trench (21) extending vertically downward through the N+ layer (15) and P layer (14)
26	providing a gate in said trench;	gate oxide layer (17)
27	wherein a deepest part of said third regions is laterally spaced from said trench;	a portion of the P layer (16) is laterally spaced from the trench (21)
21		

wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (16)
third region and said first region is less than a depletion	and the N+ layer (12) is less than a depletion width of a
width of a planar junction which has the same doping	planar junction which has the same doping profile as
profile as does said junction between said second and	does the junction between the N layer (13) and the P
third regions at said deepest part of said third region and	layer (16) at the deepest part of the P layer (16) and
which is reverse biased around its breakdown voltage.	which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ region (16)
said third region is doped heavier than a part of said	which is doped heavier than P region (14) adjacent the
third region which part is adjacent said trench	trench (21)

•	U.S. Patent 5,072,266	JP 54-57871
	CLAIM 1	
	1. A trench DMOS transistor cell comprising:	VMOS FET
	· .	See fig. 2
	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (3) and (10)
,	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (4) lying partly over the P layer (3), wherein a portion of the P layer is a heavily doped P+ (10) and
	having a top surface and partly lying over the second	extends vertically upward through the N+ layer (4) and vertically downward into the N layer (2)
	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	vertically downward into the 14 layer (2)
	vertically upward and downward, an upward portion extending through the third covering layer to the top	
	surface of the third covering layer and a downward portion extending downward into the first covering	
-	layer;	
	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer	trench (11) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (4), the P layer (3) and through a portion of the N layer (2),
	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	wherein the bottom surface of the trench (11) lies above the lowest part of the P layer (10)
	the trench lies above a lowest part of the downward portion of the second covering layer;	
	electrically conducting semiconductor material positioned within the trench;	Al gate (6) in trench (11)
	a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the	gate oxide layer (5)
	bottom and side surfaces of the trench; and	
I	three electrodes electrically coupled to the electrically	gate electrode (6), source electrode (7) and drain

U.S. Patent No. 5,298,442	JP 54-57871
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	
	See fig. 2
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type	P layer (3) and (10).
over said first region;	
providing a third region of said first conductivity type	N+ layer (4) lying above the P layer (3).
such that said first and third regions are separated by	
said second region;	
providing a trench through said third and second	the trench (11) extends through the N+ layer (4) and the
regions; and	P layer (3)
providing a gate in said trench;	Al gate (6) in trench (11)
wherein a portion P of said second region, which portion	the P layer (10) extends upward through the N+ layer
is spaced from said trench, extends deeper than said	(17) and which extends downward through the N- laye
trench so that, if a predetermined voltage is applied to	(12)
said gate and to said third region and another	
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	a portion P of the second region (10) is doped heavier
said second region is doped heavier than another portion	than another portion (3) of the second region which is
of said second region which portion is adjacent said	adjacent the trench (11)
trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)
comprises a first portion and a second portion over said	
first portion, said second portion being lighter doped	
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
breakdown is a reach-through breakdown across said	across N layer (2)
second portion.	
CLAIM 22	
21. The method of claim 17 further comprising the step	gate oxide layer (5)
of providing an insulator between said surface of said	
trench and said gate.	
CLAIM 23	
23. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	
	See fig. 2
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type	N layer (2)
over said first region, said second region being lighter	
doped than said first region;	Places (2) and (10)
providing a third region of a second conductivity type	P layer (3) and (10)
over said second region, said second and third regions	
forming a junction;	

1	providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3)
2	providing a trench through said fourth region and third regions; and	trench (11) through N+layer (4) and P layer (3)
3	providing a gate in said trench;	gate oxide film (5)
4	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (10) is laterally spaced from trench (11)
5	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (10) and the N+ layer (1) is less than a depletion width of a
6	width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and	planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer
7	which is reverse biased around its breakdown voltage.	(10) at the deepest part of the P layer (10) and which is reverse biased around its breakdown voltage
ا ہ	CLAIM 24	
8	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region (10) is doped heavier
	said third region is doped heavier than a part of said	than part (3) which is adjacent the trench (11)
9	third region which part is adjacent said trench.	

3	U.S. Patent 5,072,266	JP 57-72365
	CLAIM 1	
4	1. A trench DMOS transistor cell comprising:	VMOS FET
5		See fig. 1
	a substrate of semiconductor material of heavily doped	P+ substrate (1)
6	first electrical conductivity type;	
	a first covering layer of semiconductor material of said	N layer (2)
7	first electrical conductivity type lying on the substrate;	
	a second covering layer of semiconductor material of	P layer (3) and (4)
8	second electrical conductivity type lying on the first	
l	covering layer;	
9	a third covering layer of semiconductor material of	N+ layer (5) lying partly over the P layer (4), wherein the
	heavily doped said first electrical conductivity type and	P layer is heavily doped P+ and extends both vertically
0	having a top surface and partly lying over the second	upward through the N+ layer (5) and downward into the N layer (2)
.	covering layer, wherein a portion of the second covering	i layer (2)
1	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	
	extending through the third covering layer to the top	,
2	surface of the third covering layer and a downward	
3	portion extending downward into the first covering	
,	layer;	•
4	a trench having a bottom surface and side surfaces and	trench (6) having a bottom surface and side surfaces and
•	extending vertically downward from the top surface of	extending vertically through the N+ layer (5) and the P
5	the third covering layer through the third covering layer	layer (4), and through a portion of the N layer (2), where
	and the second covering layer and through a portion of	the bottom surface of the trench (6) lies above the lowest
5	the first covering layer, wherein the bottom surface of	part of the P layer (3)
	the trench lies above a lowest part of the downward	
7	portion of the second covering layer;	
	9 9	. 11 (0)
	electrically conducting semiconductor material positioned within the trench;	metal layer (8)

1	a layer of oxide positioned within the trench between the	gate oxide (7)
	electrically conducting semiconductor material and the	
2	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate electrode (8), source electrode (9) and drain (D)
3	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	

U.S. Patent No. 5,298,442	JP 57-72365
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	·
	See fig. 1
providing a first region of a first conductivity type;	N layer (2)
providing a second region of a second conductivity type over said first region;	P layer (4) lying over said N layer (2)
providing a third region of said first conductivity type	N+ layer (5) lying above the P layer (4)
such that said first and third regions are separated by	,
said second region;	
providing a trench through said third and second regions; and	trench (6) through the N+ layer (5) and the P layer (4)
providing a gate in said trench;	metal gate layer (8)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	a portion of the P layer (3) is spaced from the trench (6 and extends deeper than trench (6)
said gate and to said third region and another	
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of said trench.	
·	·
CLAIM 18	
18. The method of claim 17 wherein said portion P of	a portion of the second region is doped P+ (3) which is
said second region is doped heavier than another portion	heavier doped than another portion of the second regio
of said second region which portion is adjacent said	that is adjacent the trench (6)
trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	P+ layer (1) under N layer (2)
comprises a first portion and a second portion over said	
first portion, said second portion being lighter doped	
than said first portion. CLAIM 20	·
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
breakdown is a reach-through breakdown across said	across the N layer (2)
second portion. CLAIM 22	,
	gate oxide (7)
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said	Bate Oxide (1)
trench and said gate.	

1	CLAIM 23	
	23. A method for providing a transistor, said method	VMOS FET
2	comprising the steps of:	
		See fig. 1
3	providing a first region of a first conductivity type;	
	providing a second region of said first conductivity type	N layer (2)
4	over said first region, said second region being lighter	
	doped than said first region;	
5	providing a third region of a second conductivity type	P layer (4)
_	over said second region, said second and third regions	
6	forming a junction;	
7	providing a fourth region of said first conductivity type	N+ layer (5) lying above the P layer (4)
/	over said third region;	
8	providing a trench through said fourth region and third	trench (6) through the N+ layer (5) and the P layer (4).
0	regions; and	
9	providing a gate in said trench;	metal gate layer (8)
	wherein a deepest part of said third regions is laterally	the deepest part of the P layer (3) is laterally spaced from
10	spaced from said trench;	trench (6)
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (3)
11	third region and said first region is less than a depletion	and the P+ layer (1) is less than a depletion width of a
	width of a planar junction which has the same doping	planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer
12	profile as does said junction between said second and third regions at said deepest part of said third region and	(3) at the deepest part of the P layer (3) and which is
	which is reverse biased around its breakdown voltage.	reverse biased around its breakdown voltage
13	CLAIM 24	i constituente la create de la
	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is doped P+ (3) which
14	said third region is doped heavier than a part of said	is heavier doped than the part of the third region (4)
	third region which part is adjacent said trench.	adjacent the trench (6)
15		,,

1	6
1	7

U.S. Patent 5,072,266	JP 59-193064
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET
	See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (3)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top	N+ layer (5) lying partly over the P layer (4), a portion of the P layer (4) extending vertically upward through the N+ layer (5) and downward into the N layer (3)

surface of the third covering layer and a downward portion extending downward into the first covering layer; a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; 6 lectrically conducting semiconductor material positioned within the trench; 7 a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench (1) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate oxide (2) gate (8), source (7) and drain (6)		I	
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; 6 electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. trench (1) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	1	portion extending downward into the first covering	·
extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	2	layer;	
extending vertically downward from the top surface of the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)		a trench having a bottom surface and side surfaces and	trench (1) having a hottom surface and side surfaces and
the third covering layer through the third covering layer and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. the P layer (4) and a portion of the N layer (3), where the bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	3		extending vertically downward through the N+ layer (5)
and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. bottom surface of the trench (10 lies above the lowest portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)		the third covering layer through the third covering layer	the Player (4) and a portion of the N layer (3), where the
the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. portion of the P layer (4) gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	4	and the second covering layer and through a portion of	bottom surface of the trench (10 lies above the lowest
the trench lies above a lowest part of the downward portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)		the first covering layer, wherein the bottom surface of	
portion of the second covering layer; electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	5	the trench lies above a lowest part of the daymound	portion of the range (1)
electrically conducting semiconductor material positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate semiconductor material (8) in trench (1) gate oxide (2) gate (8), source (7) and drain (6)	,	portion of the second covering lever	
positioned within the trench; a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate oxide (2) gate (8), source (7) and drain (6)	_		
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate oxide (2) gate (8), source (7) and drain (6)	6		gate semiconductor material (8) in trench (1)
electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate (8), source (7) and drain (6)		positioned within the trench;	
electrically conducting semiconductor material and the bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate (8), source (7) and drain (6)	.7	a layer of oxide positioned within the trench between the	gate oxide (2)
bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering layer and to the substrate, respectively. gate (8), source (7) and drain (6)			:
conducting semiconductor material, to the third covering layer and to the substrate, respectively.	8		
conducting semiconductor material, to the third covering layer and to the substrate, respectively.		three electrodes electrically coupled to the electrically	gate (8), source (7) and drain (6)
layer and to the substrate, respectively.	9		(0)
			. •
	10		

12	` INVALIDITY CLAIM CHART FO	DIIC DATENT NO 5 200 442
13	U.S. Patent No. 5,298,442	JP 59-193064
14	CLAIM 17	
15	17. A method for providing a transistor, said method comprising the steps of:	VMOS FET
15	•	See fig. 2
16	providing a first region of a first conductivity type;	N+ layer and N layer (3)
17	providing a second region of a second conductivity type over said first region;	P layer (4) over N layer (3)
	providing a third region of said first conductivity type such that said first and third regions are separated by	N+ layer (5) lying above the P layer (4).
18	said second region;	
19	providing a trench through said third and second regions; and	trench (1) through N+ layer (5) and P layer (4)
20	providing a gate in said trench;	gate semiconductor material (8)
	wherein a portion P of said second region, which portion	a portion of the P layer (4) is spaced from trench (1) and
21	is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	extends deeper than trench (1)
22	said gate and to said third region and another predetermined voltage is applied to said first region, an	
23	avalanche breakdown occurs away from a surface of said trench.	
24	ממנע עכווניון.	
	·	
25	CLAIM 18	
26	18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier doped
	said second region is doped heavier than another portion of said second region which portion is adjacent said	P+ portion
27	trench.	

SILICON VALLEY

1	CLAIM 19	
	19. The method of claim 17 wherein said first region	N+ layer under N- layer (3)
2	comprises a first portion and a second portion over said	, (-)
	first portion, said second portion being lighter doped	
3	than said first portion.	
	CLAIM 20	
4	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
_	breakdown is a reach-through breakdown across said	across the N- layer (3)
5	second portion.	
_	CLAIM 22	
6	21. The method of claim 17 further comprising the step	gate oxide (2)
7	of providing an insulator between said surface of said	
7	trench and said gate.	
8	CLAIM 23	
0	23. A method for providing a transistor, said method	VMOS FET
9	comprising the steps of:	·
		See fig. 2
10	providing a first region of a first conductivity type;	N+ layer
10	providing a second region of said first conductivity type	N layer (3) lying above the N+ layer
11.	over said first region, said second region being lighter	
•	doped than said first region;	
12	providing a third region of a second conductivity type	P layer (4)
	over said second region, said second and third regions	
13	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer (5) lying above the P layer (4)
14	over said third region;	
	providing a trench through said fourth region and third	trench (1) through the N+ layer (5) and P layer (4)
15	regions; and	11 (2)
	providing a gate in said trench;	gate oxide (2)
16	wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of P layer (4) is laterally spaced from
		trench (1)
17	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (4)
10	third region and said first region is less than a depletion width of a planar junction which has the same doping	and the N+ layer is less than a depletion width of a planar
18	profile as does said junction between said second and	junction which has the same doping profile as does the
19	third regions at said deepest part of said third region and	junction between the N- layer (3) and the P layer (4) at
19	which is reverse biased around its breakdown voltage.	the deepest part of the P layer (4) and which is reverse biased around its breakdown voltage
20	. CLAIM 24	olased around its breakdown voltage
~~	24. The method of claim 23 wherein said deepest part of	obvious to have the second region with a having 1
21	said third region is doped heavier than a part of said	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (1)
	third region which part is adjacent said trench.	1 - portion faterally spaced from the french (1)
22		
-		

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U.S. Patent 5,072,266	JP 60-28271
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOSFET
	See fig. 3(a-h)
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)

ORRICK
HERRINGTON
& SUTCLIFFE LLP
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1	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
2	a second covering layer of semiconductor material of	P1 (0) 1(11)
2	second electrical conductivity type lying on the first	P layer (8) and (11)
3	covering layer;	
	a third covering layer of semiconductor material of	N. 1 (0) 1
4	heavily doped said first electrical conductivity type and	N+ layer (9) lying partly over the P layer (8), where a
•	having a top surface and partly lying over the second	portion of the P layer (11) extends vertically upward through the N+ layer
5	covering layer, wherein a portion of the second covering	imough the 19+ layer
_	layer is heavily doped and this portion extends both	
6	vertically upward and downward, an upward portion	
·	extending through the third covering layer to the top	
7	surface of the third covering layer and a downward	
•	portion extending downward into the first covering	
8	layer;	
	a trench having a bottom surface and side surfaces and	trench (10) having a bottom surface and side surfaces and
9	extending vertically downward from the top surface of	extending vertically downward through the N+ layer (9)
•	the third covering layer through the third covering layer	and the P layer (8) and through a portion of the N layer
10	and the second covering layer and through a portion of	(2)
	the first covering layer, wherein the bottom surface of	·
11	the trench lies above a lowest part of the downward	
	portion of the second covering layer;	
12	electrically conducting semiconductor material	poly gate (6) in trench (10)
	positioned within the trench;	,
13	a layer of oxide positioned within the trench between the	gate oxide film (5)
	electrically conducting semiconductor material and the	
14	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate (6), source (14) and drain (backside)
15	conducting semiconductor material, to the third covering	(
	layer and to the substrate, respectively.	
16		

U.S. Patent No. 5,298,442	JP 60-28271
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	VMOSFET
-	See fig. 3(a-h)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (8) and (11).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (9) lying above the P layer (8).
providing a trench through said third and second regions; and	trench (10) through N+ layer (9) and P layer (8)
providing a gate in said trench;	poly gate (6) in trench (10)

- 1		
1	wherein a portion P of said second region, which portion	a portion P of the second region (11) is spaced from the
	is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	trench (10);
	said gate and to said third region and another	the second region extends deeper than the trench (10)
	predetermined voltage is applied to said first region, an	
	avalanche breakdown occurs away from a surface of	·
4	said trench.	
5	CLAIM 10	
6 F	CLAIM 18 18. The method of claim 17 wherein said portion P of	portion P of the second region (11) is doped heavier than
	said second region is doped heavier than another portion	another portion (8) which is adjacent the trench
7	of said second region which portion is adjacent said	
	trench.	
8	CLAIM 19	
9	19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)
7	comprises a first portion and a second portion over said	
10	first portion, said second portion being lighter doped	
Ţ	than said first portion. CLAIM 20	
11	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
	breakdown is a reach-through breakdown across said	across the N layer (2)
12	second portion.	
13	CLAIM 22	-
13	21. The method of claim 17 further comprising the step	gate oxide film (5)
14	of providing an insulator between said surface of said	
_	trench and said gate.	
15	CLAIM 23	VMOSFET
	23. A method for providing a transistor, said method	VMOSFET
16	comprising the steps of:	See fig. 3(a-h)
17	providing a first region of a first conductivity type;	N+ layer (1)
17	providing a second region of said first conductivity type	N layer (2)
18	over said first region, said second region being lighter	
	doped than said first region;	
19	providing a third region of a second conductivity type	P layer (8)
	over said second region, said second and third regions	
20	forming a junction;	N+ layer (9) lying above the P layer (8)
21	providing a fourth region of said first conductivity type	N+ layer (9) lying above the r layer (6)
21	over said third region; providing a trench through said fourth region and third	trench (10) through N+ layer (9) and P layer (8)
22	regions; and	uchen (10) amough 14 any or (2) and (2)
	providing a gate in said trench;	poly gate (6) in trench (10)
23	wherein a deepest part of said third regions is laterally	deepest part of the third region is laterally spaced from
	spaced from said trench;	the trench (10)
24	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (8)
25	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a
25	width of a planar junction which has the same doping	planar junction which has the same doping profile as
26	profile as does said junction between said second and	does the junction between the N- layer (2) and the P layer (8) at the deepest part of the P layer (8) and which is
20	third regions at said deepest part of said third region and	reverse biased around its breakdown voltage
	which is reverse biased around its breakdown voltage.	TOTOLOG DIGGOG GLOUNG IN OLOGICO I TOTAL

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1	CLAIM 24	
2	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	obvious to have deepest part of the third region doped heavier than the part adjacent said trench

5 INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266 6 U.S. Patent 5,072,266 JP 57-18365 CLAIM 1 7 1. A trench DMOS transistor cell comprising: VMOS FET 8 See fig. 2 a substrate of semiconductor material of heavily doped N+ layer (1) first electrical conductivity type; a first covering layer of semiconductor material of said N layer (2) 10 first electrical conductivity type lying on the substrate; a second covering layer of semiconductor material of P layer (3) 11 second electrical conductivity type lying on the first covering layer; 12 a third covering layer of semiconductor material of N+ layer (4) lying partly over the P layer (3) heavily doped said first electrical conductivity type and 13 having a top surface and partly lying over the second covering layer, wherein a portion of the second covering 14 layer is heavily doped and this portion extends both vertically upward and downward, an upward portion 15 extending through the third covering layer to the top surface of the third covering layer and a downward 16 portion extending downward into the first covering 17 a trench having a bottom surface and side surfaces and trench (5) have a bottom surface and side surfaces which extending vertically downward from the top surface of extend vertically downward through the N+ layer (4) and 18 the third covering layer through the third covering layer the P layer (3) and through a portion of the N layer (2) and the second covering layer and through a portion of 19 in fig. 4, the P layer (2) lies between the N+ layer (4) and the first covering layer, wherein the bottom surface of the N layer (2) and extends below the bottom surface of the trench lies above a lowest part of the downward 20 the trench (5) portion of the second covering layer; electrically conducting semiconductor material gate (7) in trench (5) positioned within the trench; a layer of oxide positioned within the trench between the gate oxide layer between gate (7) and trench (5) 22 electrically conducting semiconductor material and the bottom and side surfaces of the trench; and 23 three electrodes electrically coupled to the electrically gate (7), source (6) and drain (not drawn) conducting semiconductor material, to the third covering 24 layer and to the substrate, respectively.

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U.S. Patent No. 5,298,442		JP 57-18365	
	CLAIM 17		
	17. A method for providing a transistor, said method comprising the steps of:	VMOS FET	
	tomprises at supe or .	See fig. 2	
	providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).	
	providing a second region of a second conductivity type	P layer (3).	
	over said first region;	, and the (a).	
	providing a third region of said first conductivity type	N+ layer (4) lying above the P layer (3).	
	such that said first and third regions are separated by	, , , , , , , , , , , , , , , , , , , ,	
	said second region;		
	providing a trench through said third and second regions; and	trench (5) through N+ layer (4) and P layer (3)	
	providing a gate in said trench;	gate (7) in trench (5)	
	wherein a portion P of said second region, which portion	the P layer (3) extends upward through the N+ layer (4)	
-	is spaced from said trench, extends deeper than said		
	trench so that, if a predetermined voltage is applied to	in fig. 4, P layer (4) extends deeper than trench (5)	
-	said gate and to said third region and another		
	predetermined voltage is applied to said first region, an		
	avalanche breakdown occurs away from a surface of said trench.		
	Salu uchcli.		
1	CLAIM 18		
	18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier doped	
	said second region is doped heavier than another portion	P+ portion laterally spaced from the trench (1)	
	of said second region which portion is adjacent said	- Formon mercan, spaced from the field (1)	
	trench.		
	CLAIM 19		
	19. The method of claim 17 wherein said first region	N+ layer (1) under N- layer (2)	
	comprises a first portion and a second portion over said	• •	
	first portion, said second portion being lighter doped		
1	than said first portion.		
ŀ	CLAIM 20		
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown	
	breakdown is a reach-through breakdown across said second portion.	across the N- layer (2)	
۲	CLAIM 22		
I	21. The method of claim 17 further comprising the step	gate oxide layer between gate (7) and trench (5)	
	of providing an insulator between said surface of said	Para remark and the first factor (2)	
	trench and said gate.		
	CLAIM 23		
I	23. A method for providing a transistor, said method	VMOS FET	
	comprising the steps of:		
H		See fig. 2	
H	providing a first region of a first conductivity type;	N+ layer (1)	
	providing a second region of said first conductivity type over said first region, said second region being lighter	N layer (2)	

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1 2	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3)	
3	providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3)	
4	providing a trench through said fourth region and third regions; and	trench (5) through N+ layer (4) and P layer (3)	
_	providing a gate in said trench;	gate (7) in trench (5)	
5	wherein a deepest part of said third regions is laterally spaced from said trench;	deepest part of the third region is laterally spaced from the trench (5)	
6	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (3)	
7	third region and said first region is less than a depletion width of a planar junction which has the same doping	and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as	
8	profile as does said junction between said second and third regions at said deepest part of said third region and	does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) and which is	
9	which is reverse biased around its breakdown voltage. CLAIM 24	reverse biased around its breakdown voltage	
10	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said translation.	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (7)	
11	third region which part is adjacent said trench.		

1^	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266		
14	U.S. Patent 5,072,266	JP 59-80970	
• •	CLAIM 1		
15	1. A trench DMOS transistor cell comprising:	V Groove MOSFET	
16		See fig. 2	
17	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (2)	
18	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (1)	
19	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	P layer (8)	
	covering layer;		
20	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (4) lying partly over the P layer (8), where the P	
21	having a top surface and partly lying over the second	layer (8) extends vertically upward through the N+ layer (4) and vertically downward into the N layer (1)	
22	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both		
	vertically upward and downward, an upward portion		
23	extending through the third covering layer to the top		
	surface of the third covering layer and a downward		
24	portion extending downward into the first covering layer;		
25	a trench having a bottom surface and side surfaces and	trench having a bottom surface and side surface, and	
	extending vertically downward from the top surface of	extending vertically downward through the N+ layer (4)	
26	the third covering layer through the third covering layer	and the P layer (8) and through a portion of the N layer	
	and the second covering layer and through a portion of	(1)	
27	the first covering layer, wherein the bottom surface of		
	the trench lies above a lowest part of the downward		
28	portion of the second covering layer;	·	
	DOCSSV2.600277.1		

1	electrically conducting semiconductor material positioned within the trench;	gate (6) in trench
2	a layer of oxide positioned within the trench between the	gate oxide layer (5)
2	electrically conducting semiconductor material and the	gate oxide layer (3)
3	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate (5), source (7) and drain (not drawn)
4	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	
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7	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442		
8	U.S. Patent No. 5,298,442	JP 59-80970	
ا ہ	CLAIM 17		
.9	17. A method for providing a transistor, said method	V Groove MOSFET	
10	comprising the steps of :	See fig. 2	
11	providing a first region of a first conductivity type;	N+ layer (2) and N layer (1)	
*	providing a second region of a second conductivity type	P layer (8)	
12	over said first region;	N+ layer (4) lying above the P layer (8)	
13	providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	14+ layer (4) lying above the F layer (6)	
14	providing a trench through said third and second regions; and	trench through N+ layer (4) and P layer (8)	
15	providing a gate in said trench;	gate (6) in trench	
	wherein a portion P of said second region, which portion	a portion of the P layer (8) is laterally spaced from the	
16	is spaced from said trench, extends deeper than said	trench	
	trench so that, if a predetermined voltage is applied to said gate and to said third region and another		
.17	predetermined voltage is applied to said first region, an		
18	avalanche breakdown occurs away from a surface of		
	said trench.		
19			
20	CLAIM 18		
21	18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier doped	
۷ ا	said second region is doped heavier than another portion of said second region which portion is adjacent said	P+ portion laterally spaced from the trench	
22	trench.	·	
	CLAIM 19		
23	19. The method of claim 17 wherein said first region	N+ layer (2) under N- layer (1)	
24	comprises a first portion and a second portion over said		
24	first portion, said second portion being lighter doped		
25	than said first portion.		
	CLAIM 20 20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown	
26	breakdown is a reach-through breakdown across said	avaianche breakdown is a reach-through breakdown across the N- layer (1)	
	second portion.	1	
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1	CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide layer (5)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
4	23. A method for providing a transistor, said method comprising the steps of:	V Groove MOSFET
_		See fig. 2
5	providing a first region of a first conductivity type;	N+ layer (2)
6	providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (1)
7	providing a third region of a second conductivity type	P layer (8)
8	over said second region, said second and third regions forming a junction;	T layer (6)
9	providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (8)
10	providing a trench through said fourth region and third regions; and	V trench extends through the N+ layer (4) and the P layer (3)
- 11	providing a gate in said trench;	gate (6) in the V trench
12	wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the P layer (8) is laterally spaced from the V trench
13	wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping	the distance between the deepest part of the P layer (8) and the N+ layer (2) is less than a depletion width of a planar junction which has the same doping profile as
14	profile as does said junction between said second and third regions at said deepest part of said third region and	does the junction between the N- layer (1) and the P layer (8) at the deepest part of the P layer (8) and which is
. 15	which is reverse biased around its breakdown voltage. CLAIM 24	reverse biased around its breakdown voltage
16	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench
17	third region which part is adjacent said trench.	

U.S. Patent 5,072,266	U-MOS Power FET, National Technical Report, Vol. 29(2), April 1983	
CLAIM 1		
1. A trench DMOS transistor cell comprising:	U-MOSFET – see Fig. 3 Conceptional fabrication process of U-MOSFET	
a substrate of semiconductor material of heavily doped first electrical conductivity type;	n+ layer	
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	n- layer	
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	p layer	
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	n+ layer	

	<u> </u>	
1	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	the p layer includes a p+ portion which extends upward through the n+ layer and downward into the n-layer
2	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	
3	extending through the third covering layer to the top surface of the third covering layer and a downward	
4	portion extending downward into the first covering layer;	
5	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench with a bottom surface and side surfaces which extends downward from the top surface of the n+ layer
6	the third covering layer through the third covering layer and the second covering layer and through a portion of	through the n+ layer, the p layer and through a portion of the n- layer.
7	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	
8	portion of the second covering layer;	
	electrically conducting semiconductor material	semiconductor material within the trench
9	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide positioned within the trench between the
10	electrically conducting semiconductor material and the	semiconductor material and the bottom and side surfaces
	bottom and side surfaces of the trench; and	of the trench
11	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
	conducting semiconductor material, to the third covering	material, to the top n+ layer and to the n+ substrate.
12	layer and to the substrate, respectively.	

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INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442

U-MOS Power FET, National Technical

U.S. Patent No. 5,298,442	Report, Vol. 29(2), April 1983
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	U-MOSFET – see Fig. 3 Conceptional fabrication process of U-MOSFET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type over said first region;	p layer
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	n+ layer
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward through the n+ third region, and the p second region
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	the p second region has a heavily doped p+ region which is spaced from said trench and extends deeper than said trench

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said trench.

1	CLAIM 18	
	18. The method of claim 17 wherein said portion P of	the p second region contains a portion P which is doped
2	said second region is doped heavier than another portion	heavier than another portion of said second region which
	of said second region which portion is adjacent said	is adjacent said trench
3	trench.	·
	CLAIM 19	
4	19. The method of claim 17 wherein said first region	the first region comprises a n+ layer substrate (first
	comprises a first portion and a second portion over said	portion) and a n- layer (second portion)
5	first portion, said second portion being lighter doped	
	than said first portion.	
6	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
. 7	breakdown is a reach-through breakdown across said	across the n- layer (second portion) of the first region
	second portion.	
8	CLAIM 22	
	21. The method of claim 17 further comprising the step	oxide positioned within the trench between the
9	of providing an insulator between said surface of said	semiconductor material and the bottom and side surfaces
	trench and said gate.	of the trench
10	CLAIM 23	
11	23. A method for providing a transistor, said method	U-MOSFET – see Fig. 3 Conceptional fabrication
- 11	comprising the steps of:	process of U-MOSFET
12	providing a first region of a first conductivity type;	n+ layer
	providing a second region of said first conductivity type	n- layer
13	over said first region, said second region being lighter	·
	doped than said first region;	
14	providing a third region of a second conductivity type	p layer over n- layer
	over said second region, said second and third regions	·
15	forming a junction;	
	providing a fourth region of said first conductivity type	n+ layer formed over the p layer
16	over said third region; providing a trench through said fourth region and third	Annah autondina dayanyand thayyah tha nel layar (fayyah
	regions; and	trench extending downward through the n+ layer (fourth region) and the p layer (third region)
17	providing a gate in said trench;	gate electrode in the trench
18	wherein a deepest part of said third regions is laterally	the deepest part of the p layer (third region) is laterally
10	spaced from said trench;	spaced from the trench
19	wherein a distance between said deepest part of said	opwood irom tiro trouve
-	third region and said first region is less than a depletion	·
20	width of a planar junction which has the same doping	
	profile as does said junction between said second and	
21	third regions at said deepest part of said third region and	
	which is reverse biased around its breakdown voltage.	
22	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	the deepest part of the p layer (third region) is doped
23	said third region is doped heavier than a part of said	heavier (p+) than the part of the p layer (third region)
	third region which part is adjacent said trench.	adjacent the trench
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U.3	5. Patent 5,072,266	КАТОН
	CLAIM 1	
1. A trench DMOS	transistor cell comprising:	Design of New Structural High Breakdown Voltage V- MOSFET—Static Shield V-MOSFET
		Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
first electrical cond	conductor material of heavily doped uctivity type;	n+ layer
first electrical condi	er of semiconductor material of said uctivity type lying on the substrate;	n- layer
a second covering la second electrical co covering layer;	ayer of semiconductor material of nductivity type lying on the first	p layer
heavily doped said f having a top surface	er of semiconductor material of first electrical conductivity type and and partly lying over the second	n+ layer
covering layer, when layer is heavily dope	rein a portion of the second covering ed and this portion extends both	
extending through th	nd downward, an upward portion ne third covering layer to the top	
surface of the third of portion extending do layer;	covering layer and a downward ownward into the first covering	
	ttom surface and side surfaces and	
extending vertically the third covering lay	downward from the top surface of yer through the third covering layer	trench extends downward from the top surface of the n+ layer through the n+ layer, the p layer and through a portion of the n- layer.
and the second cover the first covering lay	ring layer and through a portion of er, wherein the bottom surface of	
the trench lies above portion of the second	a lowest part of the downward I covering layer;	
positioned within the	ng semiconductor material trench;	semiconductor material within the trench
electrically conductir	tioned within the trench between the ng semiconductor material and the	oxide positioned within the trench between the semiconductor material and the bottom and side surfaces
three electrodes alact	aces of the trench; and rically coupled to the electrically	of the trench
conducting semicond layer and to the subst	luctor material, to the third covering	three electrodes electrically coupled to the semiconducto material, to the top n+ layer and to the n+ substrate.

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U.S. Patent No. 5,298,442	КАТОН
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Design of New Structural High Breakdown Voltage V- MOSFET—Static Shield V-MOSFET
	Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type over said first region;	p layer
providing a third region of said first conductivity type such that said first and third regions are separated by	n+ layer
said second region;	
providing a trench through said third and second regions; and	trench extends through the n+ layer (third region) and p layer (second region)
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the p second region has a portion which is spaced from said trench and extends deeper than said trench
trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of said trench.	·
CLAIM 18	
18. The method of claim 17 wherein said portion P of	N/A
said second region is doped heavier than another portion of said second region which portion is adjacent said	
trench.	
CLAIM 19	Al- Fire and a second of the s
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	the first region comprises a n+ layer substrate (first portion) and a n- layer (second portion)
first portion, said second portion being lighter doped than said first portion.	
CLAIM 20	avalancha basaladama is a sasab at a sa ta ta a 1.1
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the n- layer (second portion) of the first region
CLAIM 22	
	oxide positioned within the trench between the
21. The method of claim 17 further comprising the step of providing an insulator between said surface of said	
of providing an insulator between said surface of said trench and said gate.	of the trench
of providing an insulator between said surface of said trench and said gate. CLAIM 23 23. A method for providing a transistor, said method	of the trench Design of New Structural High Breakdown Voltage V-
of providing an insulator between said surface of said trench and said gate. CLAIM 23	

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	providing a second region of said first conductivity type over said first region, said second region being lighter	n- layer
:	doped than said first region;	
	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	p layer over n- layer
	providing a fourth region of said first conductivity type over said third region;	n+ layer formed over the p layer
	providing a trench through said fourth region and third regions; and	trench extending downward through the n+ layer (fourth region) and the p layer (third region)
	providing a gate in said trench;	gate electrode in the trench
	wherein a deepest part of said third regions is laterally spaced from said trench;	the deepest part of the p layer (third region) is laterally spaced from the trench
	wherein a distance between said deepest part of said third region and said first region is less than a depletion	
	width of a planar junction which has the same doping profile as does said junction between said second and	
	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	
	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	N/A
	said third region is doped heavier than a part of said	
∦	third region which part is adjacent said trench.	

Prior Art Under 35 U.S.C. § 103 Which Render the '266 and '442 Patents Obvious:

U.S. Patent 4,345,265 in combination with U.S. Patent 4,374,455

U.S. Patent 4,443,931 in combination with U.S. Patent 4,374,455

U.S. Patent 4,532,534 in combination with U.S. Patent 4,374,455

U.S. Patent 4,345,265 in combination with U.S. Patent 4,767,722

U.S. Patent 4,783,694 in combination with U.S. Patent 3,412,297

U.S. Patent 4,593,302 in combination with U.S. Patent 3,412,297

(Multiple alternative combinations using the prior art references combined above can be made which additionally render the '266 and '442 patents obvious)

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2	INVALIDITY CLAIM CHART FOI	U.S. Patent 4,345,265
3	U.S. Patent 5,072,266	In Combination With U.S. Patent 4,374,455
	CLAIM 1	
4 1	1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
6		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
- 11	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '455 Patent: Fig. 2: N+ layer (34)
8 a	a first covering layer of semiconductor material of said	'265 Patent: Figs. 4-6: N- layer (12)
	first electrical conductivity type lying on the substrate;	3
9 L		'455 Patent: Fig. 2: N- layer (36)
0 s	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
1 L		'455 Patent: Fig. 2: P layer (52) and (54)
2 a	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
3 0	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both
Н.	vertically upward and downward, an upward portion	vertically upward and downward; an upward portion of
5 s	extending through the third covering layer to the top surface of the third covering layer and a downward	the P+ region extends through the N+ layer (32) and (34) and a downward portion extends downward into the N-layer (12).
F	portion extending downward into the first covering ayer;	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
7		layer (52) and (54)
8		'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically
9		upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
		downward portion extends downward in the N- layer (36).
1 e	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	'455 Patent: Fig. 2: groove (42) having a bottom surface and side surfaces and extending vertically downward
2 a	the third covering layer through the third covering layer and the second covering layer and through a portion of	from the N+ layer (40) through the N+ layer (40) and the P layer (52) and through a portion of the N- layer (36).
3 t	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	'265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point
∡ اــُ		of the grove (42) of the '455 patent
, 1	electrically conducting semiconductor material positioned within the trench;	'455 Patent: Fig. 2: electrode (49)
ء ا ء	a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the	'455 Patent: Fig. 2: oxide layer (47) within the groove (42)
7 t	bottom and side surfaces of the trench; and three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	'455 Patent: Fig. 2: source electrodes (58), drain electrode (50) and gate electrode (49).
	layer and to the substrate, respectively.	otonione (50) and Bate otonione (45).

1	INVALIDITY CLAIM CHART FOR	R U.S. PATENT NO. 5,298,442
2 3	U.S. Patent No. 5,298,442	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,374,455
Ī	CLAIM 17	
4 5	17. A method for providing a transistor, said method comprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
6		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
7	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12)
8	providing a second region of a second conductivity type over said first region;	'455 Patent: Fig. 2: N+ layer (34) and N- layer (36) '265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23); Col. 3, ln. 42.
9		'455 Patent: Fig. 2: P layer (52) and (54)
10	providing a third region of said first conductivity type such that said first and third regions are separated by	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
11	said second region;	'455 Patent: Fig. 2: N+ layer (40)
12	providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
13	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
14	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'265 Patent: Col. 5, lns. 32-47 - "The effect of regions 21 and 23 in enhancing the breakdown characteristic of the
15	trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an	DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external periphery of or beneath regions 21 and 22 diverts breakdown from
16	avalanche breakdown occurs away from a surface of said trench.	the sensitive channel regions of the DMOS device in the P- regions under the gate 24."
17 18	•	'265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (42) of the '455 patent
	CLAIM 18	
19	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically
20 21	of said second region which portion is adjacent said trench.	upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a downward portion extends downward in the N- layer
22		(36).
23		'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and
24		(23) are more heavily doped than P- region (20) and (22) near the gate region.
25	CLAIM 19	
26	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	'455 patent: Fig. 2: N+ layer (34) under N- layer (36) '265 Patent: Figs. 4-6: N+ layer (10) under N- layer (12)
27	first portion, said second portion being lighter doped than said first portion.	203 Fatent. Figs. 4-0; 147 layer (10) under 14- layer (12)

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1	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	'265 Patent and '455 Patent: avalanche breakdown
2	breakdown is a reach-through breakdown across said	would be a reach-through breakdown across the N- layer
ŀ	second portion.	(12)
3	CLAIM 22	
Ì	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
4	of providing an insulator between said surface of said	` ,
	trench and said gate.	
5	CLAIM 23	
l	23. A method for providing a transistor, said method	'265 Patent: MOS Power Transistor With Improved
6	comprising the steps of:	High-Voltage Capability
ļ	comprising the steps of	
7		'455 Patent: Method for Manufacturing a Vertical,
		Grooved MOSFET
8	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
ļ	providing a first region of a first conductivity type,	
9		'455 Patent: Fig. 2: N+ layer (34)
Ì	providing a second region of said first conductivity type	'265 Patent: Figs. 4-6: N- layer (12)
10	over said first region, said second region being lighter	
	doped than said first region;	'455 Patent: Fig. 2: N- layer (36)
11	providing a third region of a second conductivity type	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
	over said second region, said second and third regions	over the second region
12	forming a junction;	
		'455 Patent: Fig. 2: P layer (52)
13	providing a fourth region of said first conductivity type	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly
	over said third region;	lying over P- layer (20) and (22).
14	<u>.</u>	March 1 Ti O Mart 1 (40) of 1 in any D
		'455 Patent: Fig. 2: N+ layer (40) partly lying over P
15		layer (52)
	providing a trench through said fourth region and third	'455 Patent: Fig. 2: groove (42) through the N+ layer
16	regions; and	(40) and the P layer (52)
	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
17	wherein a deepest part of said third regions is laterally	'265 Patent: Figs. 4-6: P+ region (21) and (23) is
	spaced from said trench;	laterally spaced from the gate
18	wherein a distance between said deepest part of said	'265 and '455: a distance between said deepest part of a
,	third region and said first region is less than a depletion	third region and a first region would be less than a
19	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
	profile as does said junction between said second and	doping profile as does said junction between a second
20	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
۱, ۱	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
21	CI ADV 24	voltage.
22	CLAIM 24	1965 Para A Fina A Granadian Saha P Jananian
22	24. The method of claim 23 wherein said deepest part of	'265 Patent: Figs. 4-6: a portion of the P- layer is a
23	said third region is doped heavier than a part of said	heavily doped P+ region (21) and (23) and extends both
23	third region which part is adjacent said trench.	vertically upward and downward; P+ region (21) and
24		(23) are more heavily doped than P- region (20) and (22)
2 -7		near the gate region.

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	U.S. Patent 5,072,266	U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455
_	CLAIM 1	
]	1. A trench DMOS transistor cell comprising:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion
		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
f	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'931 Patent: Fig. 13: N+ layer (12)
1	a first covering layer of semiconductor material of said	'455 Patent: Fig. 2: N+ layer (34)
f	Tirst electrical conductivity type lying on the substrate;	'931 Patent: Fig. 13: N layer (14)
\perp		'455 Patent: Fig. 2: N- layer (36)
a	second covering layer of semiconductor material of	'931 Patent: Fig. 13: P layer (34) and (28)
	econd electrical conductivity type lying on the first	
-	overing layer;	'455 Patent: Fig. 2: P layer (52) and (54)
h	third covering layer of semiconductor material of leavily doped said first electrical conductivity type and laving a top surface and partly lying over the second	'931 Patent: Fig. 13: N+ layer (36) partly lying over F layer (34) and (28).
L.	overing layer, wherein a portion of the second covering	'031 Patenti Fig. 12: a martian and D.L. (24)
la	ayer is heavily doped and this portion extends both	'931 Patent: Fig. 13: a portion of the P layer (34) is a heavily doped P+ region (28) and extends both vertical
v	ertically upward and downward, an upward portion	upward and downward; an upward portion of the P+
e	xtending through the third covering layer to the top	region extends through the N+ layer (38) and a
รเ	urface of the third covering layer and a downward	downward portion extends downward into the N layer
po	ortion extending downward into the first covering	(14).
la	yer;	
		'455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52) and (54)
		'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertical
		upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
		downward portion extends downward to the N- layer (36).
ex	trench having a bottom surface and side surfaces and stending vertically downward from the top surface of third covering layer through the third covering layer	'455 Patent: Fig. 2: groove (42) having a bottom surfact and side surfaces and extending vertically downward from the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer (40) and the N+ layer (40) and the N+ layer (40) through the N+ layer (40) and the N+ layer
an	nd the second covering layer and through a portion of e first covering layer, wherein the bottom surface of	P layer (52) and through a portion of the N- layer (36).
the	e trench lies above a lowest part of the downward	
p0	ortion of the second covering layer;	
po	ectrically conducting semiconductor material sitioned within the trench;	'455 Patent: Fig. 2: electrode (49)
ele	layer of oxide positioned within the trench between the ectrically conducting semiconductor material and the ottom and side surfaces of the trench; and	'455 Patent: Fig. 2: oxide layer (47) within the groove (42)
	ree electrodes electrically coupled to the electrically	455 Potenti Fig. 2. compa -1 1 (50) 1
CO	inducting semiconductor material, to the third covering	'455 Patent: Fig. 2: source electrodes (58), drain
	yer and to the substrate, respectively.	electrode (50) and gate electrode (49).

U.S. Patent No. 5,298,442	U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion
	'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12) and N layer (14)
	'455 Patent: Fig. 2: N+ layer (34) and N- layer (36)
providing a second region of a second conductivity type over said first region;	'931 Patent: Fig. 13: P layer (34) and (28)
	'455 Patent: Fig. 2: P layer (52)
providing a third region of said first conductivity type	'931 Patent: Fig. 13: N+ layer (12) partly lying over P
such that said first and third regions are separated by said second region;	layer (34)
	'455 Patent: Fig. 2: N+ layer (40)
providing a trench through said third and second	'455 Patent: Fig. 2: groove (42) extending vertically
regions; and	downward through the N+ layer (40) and the P layer (5
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
wherein a portion P of said second region, which portion	'931 patent and '455 patent: the deep P+ region (28) of
is spaced from said trench, extends deeper than said	the '931 patent would be below the lowest point of the
trench so that, if a predetermined voltage is applied to	grove (42) of the '455 patent
said gate and to said third region and another predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CLATA 10	
CLAIM 18	1001 P
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'931 Patent: Fig. 13: a portion of the P layer (34) is a heavily doped P+ region (28)
of said second region which portion is adjacent said trench.	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertical
	upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
-	downward portion extends downward in the N- layer (36).
CLAIM 19	(30).
19. The method of claim 17 wherein said first region	'455 patent: Fig. 2: N+ layer (34) under N- layer (36)
comprises a first portion and a second portion over said	
first portion, said second portion being lighter doped	'931 Patent: Fig. 13: N+ layer (12) under N- layer (14)
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	'931 Patent and '455 Patent: avalanche breakdown
breakdown is a reach-through breakdown across said second portion.	would be a reach-through breakdown across the N- layer (12)

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1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
2	of providing an insulator between said surface of said	· ·
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'931 Patent: Method of Fabricating a Semiconductor
4	comprising the steps of:	Device With a Base Region Having a Deep Portion
_		
5		'455 Patent: Method for Manufacturing a Vertical,
6		Grooved MOSFET
0	providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12)
7		'455 Patent: Fig. 2: N+ layer (34)
	providing a second region of said first conductivity type	'931 Patent: Fig. 13: N layer (14)
8	over said first region, said second region being lighter	
	doped than said first region;	'455 Patent: Fig. 2: N- layer (36)
9	providing a third region of a second conductivity type	'931 Patent: Fig. 13: P layer (34) and (28)
	over said second region, said second and third regions	
10	forming a junction;	'455 Patent: Fig. 2: P layer (52)
	providing a fourth region of said first conductivity type	'931 Patent: Fig. 13: N+ layer (36) partly lying over P
11	over said third region;	layer (34) and (28)
12	,	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
12		layer (52)
13	providing a trench through said fourth region and third	'455 Patent: Fig. 2: groove (42) through the N+ layer
	regions; and	(40) and the P layer (52)
14	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
	wherein a deepest part of said third regions is laterally	'931 Patent: Fig. 13: P+ region (28) is laterally spaced
15	spaced from said trench;	from the gate
	wherein a distance between said deepest part of said	'931 and '455: a distance between said deepest part of a
16	third region and said first region is less than a depletion	third region and a first region would be less than a
.,	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
17	profile as does said junction between said second and	doping profile as does said junction between a second
18	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
10	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
19	CLAIM 24	voltage.
•		(021 Passat, Fig. 12. a page Cat- Pl i - 1
20	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said	'931 Patent: Fig. 13: a portion of the Player is a heavily
·	third region which part is adjacent said trench.	doped P+ region (28) and extends both vertically upward and downward; P+ region (28) is more heavily doped
21	ding region which part is adjacent said hench.	than P- region (34) near the gate region.
		man 1 - region (34) near me gate region.

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2	U.S. Patent 5,072,266	U.S. Patent 4,532,534 In Combination With U.S. Patent4,374,455
3	CLAIM 1	U.S. Patent4,574,455
	1. A trench DMOS transistor cell comprising:	'534 Patent: MOSFET With Perimeter Channel
		(ACCD - ACAD - ACCD - A
		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
	a substrate of semiconductor material of heavily doped	'534 Patent: Fig. 2: N+ layer (118)
,	first electrical conductivity type;	'455 Patent: Fig. 2: N+ layer (34)
	a first covering layer of semiconductor material of said	'534 Patent: Fig. 2: N- layer (120)
}	first electrical conductivity type lying on the substrate;	
•	, , , , , , , , , , , , , , , , , , , ,	'455 Patent: Fig. 2: N- layer (36)
	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	'534 Patent: Fig. 2: P layer (124) and (126)
) .	covering layer;	'455 Patent: Fig. 2: P layer (52) and (54)
,.	a third covering layer of semiconductor material of	'534 Patent: Fig. 2: N+ layer (128) partly lying over P
l	heavily doped said first electrical conductivity type and	layer (124) and (126)
	having a top surface and partly lying over the second	
	covering layer, wherein a portion of the second covering	'534 Patent: Fig. 2: a portion of the P layer is a heavily
	layer is heavily doped and this portion extends both	doped P+ region (126) and extends both vertically
	vertically upward and downward, an upward portion	upward and downward; an upward portion of the P+
	extending through the third covering layer to the top	region extends through the N+ layer (128) and a downward portion extends downward into the N- layer
	surface of the third covering layer and a downward	(120).
	portion extending downward into the first covering	(120).
;	layer;	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
_		layer (52) and (54)
5		'455 Patent: Fig. 2: a portion of the P layer (52) is a
7		heavily doped P+ region (54) and extends both vertically
	·	upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
3		downward portion extends downward to the N- layer
		(36).
)	a trench having a bottom surface and side surfaces and	'455 Patent: Fig. 2: groove (42) having a bottom surface
)	extending vertically downward from the top surface of	and side surfaces and extending vertically downward
,	the third covering layer through the third covering layer	from the N+ layer (40) through the N+ layer (40) and the
l	and the second covering layer and through a portion of	P layer (52) and through a portion of the N- layer (36).
	the first covering layer, wherein the bottom surface of	
2	the trench lies above a lowest part of the downward	
	portion of the second covering layer;	
,	electrically conducting semiconductor material	'455 Patent: Fig. 2: electrode (49)
	positioned within the trench;	
ļ	a layer of oxide positioned within the trench between the	'455 Patent: Fig. 2: oxide layer (47) within the groove
	electrically conducting semiconductor material and the	(42)
5	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	'455 Patent: Fig. 2: source electrodes (58), drain
5	conducting semiconductor material, to the third covering	electrode (50) and gate electrode (49).
	layer and to the substrate, respectively.	

Į	INVALIDITY CLAIM CHART FOR	
2 3	U.S. Patent No. 5,298,442	U.S. Patent 4,443,534 In Combination With U.S. Patent 4,374,455
-	CLAIM 17	
4	17. A method for providing a transistor, said method comprising the steps of:	'534 Patent: MOSFET With Perimeter Channel
5	•	'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
6	providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118) and N layer (120)
7		'455 Patent: Fig. 2: N+ layer (34) and N- layer (36)
8	providing a second region of a second conductivity type over said first region;	'534 Patent: Fig. 2: P layer (124) and (126)
		'455 Patent: Fig. 2: P layer (52)
9	providing a third region of said first conductivity type such that said first and third regions are separated by	'534 Patent: Fig. 2: N+ layer (128) partly lying over P layer (124) and (126)
10	said second region;	'455 Patent: Fig. 2: N+ layer (40)
11	providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
12	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'534 patent and '455 patent: the deep P+ region (126) of the '534 patent would be below the lowest point of the-
13	trench so that, if a predetermined voltage is applied to said gate and to said third region and another	grove (42) of the '455 patent
14	predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
15	said trench.	
16		
17	CLAIM 18	Colonia Pi 10 colonia Piccolo
18	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'534 Patent: Fig. 12: a portion of the P layer is a heavily doped P+ region (126)
19	of said second region which portion is adjacent said trench.	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically
20		upward and downward; an upward portion of the P+
20		region extends through the N+ layer (40) and a
		region extends through the N+ layer (40) and a downward portion extends downward in the N- layer (36).
20 21 22	CLAIM 19 19. The method of claim 17 wherein said first region	downward portion extends downward in the N- layer
21	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	downward portion extends downward in the N- layer (36).
21 22 23	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped	downward portion extends downward in the N- layer (36). '455 patent: Fig. 2: N+ layer (34) under N- layer (36)
21 22	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.	downward portion extends downward in the N- layer (36). '455 patent: Fig. 2: N+ layer (34) under N- layer (36) '534 Patent: Fig. 2: N+ layer (118) under N- layer (120)
21 22 23	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped	downward portion extends downward in the N- layer (36). '455 patent: Fig. 2: N+ layer (34) under N- layer (36)

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1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'534 Patent: Method of Fabricating a Semiconductor
4	comprising the steps of:	Device With a Base Region Having a Deep Portion
5		'455 Patent: Method for Manufacturing a Vertical,
		Grooved MOSFET
6	providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118)
7		'455 Patent: Fig. 2: N+ layer (34)
8	providing a second region of said first conductivity type over said first region, said second region being lighter	'534 Patent: Fig. 2: N- layer (120)
	doped than said first region;	'455 Patent: Fig. 2: N- layer (36)
, 9	providing a third region of a second conductivity type over said second region, said second and third regions	'534 Patent: Fig. 2: P layer (124) and (126)
10	forming a junction;	'455 Patent: Fig. 2: P layer (52)
11	providing a fourth region of said first conductivity type over said third region;	'534 Patent: Fig. 2: N+ layer (128) partly lying over P layer (124) and (126)
	over said time region,	1, 0 (-2.)
12.	•	'455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52)
	11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	'455 Patent: Fig. 2: groove (42) through the N+ layer
13	providing a trench through said fourth region and third	(40) and the P layer (52)
	regions; and	
14	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
1.5	wherein a deepest part of said third regions is laterally	'534 Patent: Figs. 4-6: P+ region (126) is laterally spaced from the gate
15	spaced from said trench;	
,,	wherein a distance between said deepest part of said	'534 and '455: a distance between said deepest part of a
16	third region and said first region is less than a depletion	third region and a first region would be less than a
17	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
17	profile as does said junction between said second and	doping profile as does said junction between a second
10	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
18	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown voltage.
19	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	'534 Patent: Figs. 4-6: a portion of the P layer is a
20	said third region is doped heavier than a part of said	heavily doped P+ region (126) and extends both
	third region which part is adjacent said trench.	vertically upward and downward; P+ region (126) is
21		more heavily doped than P region (124) which is near the gate region.
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U.S. Patent 5,072,266	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,767,722
CLAIM 1	·
1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
	'722 Patent: Method for Making Planar Vertical Cha DMOS Structures
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
	'722 Patent: Figs. 6 and 8: N+ layer (10)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'265 Patent: Figs. 4-6: N- layer (12)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first	'722 Patent: Figs. 6 and 8: N- layer (11) '265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (
covering layer;	'722 Patent: Figs. 6 and 8: P layer (20a)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends be vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (32) and (and a downward portion extends downward into the N layer (12).
layer;	'722 Patent: Figs. 6 and 8: N+ layer (21a) partly lyin over P layer (20a)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer	'722 Patent: Figs. 6 and 8: groove (31) having a botto surface and side surfaces and extending vertically downward from the N+ layer (21a) through the N+ la
and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	(21a) and the P layer (20a) and through a portion of the N-layer (11).
the trench lies above a lowest part of the downward portion of the second covering layer;	'265 patent and '455 patent: the deep P+ region (21) a (23) of the '265 patent would be below the lowest poi of the grove (42) of the '455 patent
electrically conducting semiconductor material positioned within the trench;	'722.Patent: Figs. 6 and 8: gate (34)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	'722 Patent: Figs. 6 and 8: oxide layer (32) within the groove (31)
three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	'722 Patent: Fig. 6 and 8: source electrodes (50), drain electrode (51) and gate electrode (49).

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	INVALIDITY CLAIM CHART FOR	U.S. Patent 4,345,265
	U.S. Patent No. 5,298,442	In Combination With U.S. Patent 4,767,722
	CLAIM 17	
II.	. A method for providing a transistor, said method mprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
		'722 Patent: Method for Making Planar Vertical Chann DMOS Structures
pro	oviding a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12)
		'722 Patent: Figs. 6 and 8: N+ layer (10) and N- layer (11)
	oviding a second region of a second conductivity type er said first region;	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23 Col. 3, ln. 42.
		'722 Patent: Figs. 6 and 8: P layer (20a)
suc	oviding a third region of said first conductivity type ch that said first and third regions are separated by	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
	d second region;	'722 Patent: Figs. 6 and 8: N+ layer (21a)
	oviding a trench through said third and second gions; and	'722 Patent: Figs. 6 and 8: groove (31) extending vertically downward through the N+ layer (21a) and the P layer (20a)
pro	oviding a gate in said trench;	'722 Patent: Figs. 6 and 8: gate (34) in groove (31)
wh is s tres sai pre ava	derein a portion P of said second region, which portion spaced from said trench, extends deeper than said nch so that, if a predetermined voltage is applied to id gate and to said third region and another edetermined voltage is applied to said first region, an alanche breakdown occurs away from a surface of id trench.	'265 Patent: Col. 5, Ins. 32-47 – "The effect of regions and 23 in enhancing the breakdown characteristic of the DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external periphery of or beneath regions 21 and 22 diverts breakdown from the sensitive channel regions of the DMOS device in the P- regions under the gate 24."
		'265 patent and '722 patent: the deep P+ region (21) ar (23) of the '265 patent would be below the lowest poin of the grove (31) of the '722 patent
┢	CLAIM 18	
sai of	The method of claim 17 wherein said portion P of id second region is doped heavier than another portion said second region which portion is adjacent said each.	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends bot vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (2 pear the gate region
	CT ATM 10	near the gate region.
	CLAIM 19 The method of claim 17 wherein said first region emprises a first portion and a second portion over said	'722 patent: Figs. 6and 8: N+ layer (10) under N- layer (11)
fir	est portion, said second portion being lighter doped an said first portion.	'265 Patent: Figs. 4-6: N+ layer (10) under N- layer (1
-	CLAIM 20	
11	D. The method of claim 19 wherein said avalanche eakdown is a reach-through breakdown across said cond portion.	'265 Patent and '722 Patent: avalanche breakdown would be a reach-through breakdown across the N- lay (11) of the '722 Patent

1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'722 Patent: oxide (32)
2	of providing an insulator between said surface of said	·
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'265 Patent: MOS Power Transistor With Improved
4	comprising the steps of:	High-Voltage Capability
~	1	
5		'722 Patent: Method for Making Planar Vertical Channel
6		DMOS Structures
U	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
. 7		
		'722 Patent: Figs. 6 and 8: N+ layer (10)
8	providing a second region of said first conductivity type	'265 Patent: Figs. 4-6: N- layer (12)
_	over said first region, said second region being lighter	(700 Beauty Fire Cond 9, N. Janes (11)
9	doped than said first region;	'722 Patent: Figs. 6 and 8: N- layer (11)
	providing a third region of a second conductivity type	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
10	over said second region, said second and third regions	over the second region
	forming a junction;	'722 Patent: Figs. 6 and 8: P layer (20a)
11	providing a fourth region of said first conductivity type	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly
	over said third region;	lying over P- layer (20) and (22).
12		
13		'722 Patent: Fig. 6 and 8: N+ layer (21a) partly lying
13		over P layer (20a)
14	providing a trench through said fourth region and third	'722 Patent: Figs. 6 and 8: groove (31) through the N+
- 1	regions; and	layer (21a) and the P layer (20a)
15	providing a gate in said trench;	'722 Patent: Figs. 6 and 8: gate (34) '265 Patent: Figs. 4-6: P+ region (21) and (23) is
	wherein a deepest part of said third regions is laterally spaced from said trench;	laterally spaced from the gate
16	wherein a distance between said deepest part of said	'265 and '722: a distance between said deepest part of a
	third region and said first region is less than a depletion	third region and a first region would be less than a
17	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
	profile as does said junction between said second and	doping profile as does said junction between a second
18	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
10	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
19	<u> </u>	voltage.
20	CLAIM 24	
20	24. The method of claim 23 wherein said deepest part of	'265 Patent: Figs. 4-6: a portion of the P- layer is a
21	said third region is doped heavier than a part of said	heavily doped P+ region (21) and (23) and extends both
	third region which part is adjacent said trench.	vertically upward and downward; P+ region (21) and
22	<u> </u>	(23) are more heavily doped than P- region (20) and (22)
		near the gate region.
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2	U.S. Patent 5,072,266	U.S. Patent 4,783,694 In Combination With
3		U.S. Patent 3,412,297
	CLAIM 1	
4	1. A trench DMOS transistor cell comprising:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain
5		Device with Continuit Confector and Drain
•		'297 Patent: MOS Field-Effect Transistor with a One-
6		Micron Vertical Channel
	a substrate of semiconductor material of heavily doped	'694 Patent: Fig. 5: N substrate (40c)
7	first electrical conductivity type;	
	a first covering layer of semiconductor material of said	'694 Patent: Fig. 5: N-Epi layer (40)
8	first electrical conductivity type lying on the substrate;	·
_		'297 Patent: Figs. 4-6: N layer (10)
9	a second covering layer of semiconductor material of	'694 Patent: Fig. 5: P layer (42), (42a) and (42e)
^	second electrical conductivity type lying on the first	(207 Potent: Figs. 4.6: P. lover (12)
0	covering layer;	'297 Patent: Figs. 4-6: P layer (12)
1	a third covering layer of semiconductor material of	'694 Patent: Fig. 5: N+ layer (44) partly lying over P layer (42a) and (42e) where a portion of the P layer (42e)
٠.	heavily doped said first electrical conductivity type and having a top surface and partly lying over the second	is heavily doped P+ and extends vertically upward
2	covering layer, wherein a portion of the second covering	through the N+ layer (44) and vertically downward into
•	layer is heavily doped and this portion extends both	the N-Epi layer (40)
3	vertically upward and downward, an upward portion	
	extending through the third covering layer to the top	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
4	surface of the third covering layer and a downward	layer (12)
	portion extending downward into the first covering	·
5	layer;	
	a trench having a bottom surface and side surfaces and	'297 Patent: Figs 4-6: trench (18) extends downward
5	extending vertically downward from the top surface of	from the top surface of the N layer (16) through the N
,	the third covering layer through the third covering layer	layer (16), P layer (12) and through a portion of the N
7	and the second covering layer and through a portion of	layer (10)
8	the first covering layer, wherein the bottom surface of	
י כ	the trench lies above a lowest part of the downward	
9	portion of the second covering layer; electrically conducting semiconductor material	'297 Patent: conductive semiconductor material (24)
	positioned within the trench;	257 I atent. conductive semiconductor material (24)
0	a layer of oxide positioned within the trench between the	'297 Patent: oxide (14)
	electrically conducting semiconductor material and the	
1	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	'694 Patent: gate (47), source (36) and drain (40c)
2	conducting semiconductor material, to the third covering	
3	layer and to the substrate, respectively.	'297 Patent: electrodes coupled to the gate (24), source (22) and drain (20)

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1	INVALIDITY CLAIM CHART FOI	R U.S. PATENT NO. 5,298,442
2	U.S. Patent No. 5,298,442	U.S. Patent 4,783,694 In Combination With U.S. Patent 3,412,297
	CLAIM 17	
4	17. A method for providing a transistor, said method comprising the steps of:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain
6		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
7	providing a first region of a first conductivity type;	'694 Patent: Fig. 5: N-Epi layer (40).
<i>'</i>		'297 Patent: Figs. 4-6: N layer (10)
8	providing a second region of a second conductivity type over said first region;	'694 Patent: Fig. 5: P layer (42), (42a) and (42e) lying over the N-Epi layer (40)
9.		'297 Patent: Figs. 4-6: P layer (12)
10	providing a third region of said first conductivity type such that said first and third regions are separated by	'694 Patent: Fig. 5: N+ layer (44) partly lying over P layer (42a) and (42e)
11	said second region;	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
12	providing a trench through said third and second	layer (12) '297 Patent: Figs. 4-6: trench (18) through the N layer (16) and the P layer (12)
13	regions; and providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
	wherein a portion P of said second region, which portion	'694 patent and '297 patent: the deep P+ region (42e) of
14	is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	the '694 patent would be below the lowest point of the trench (18) of the '297 patent
15	said gate and to said third region and another predetermined voltage is applied to said first region, an	
16	avalanche breakdown occurs away from a surface of said trench.	
17		
18	CLAIM 18	
19	18. The method of claim 17 wherein said portion P of	'694 Patent: Fig. 5: a portion of the P layer is a heavily
20	said second region is doped heavier than another portion of said second region which portion is adjacent said	doped P+ region (42e); the P+ region (42e) is doped heavier than the P region (42a) adjacent the gate region.
21	trench.	
	CLAIM 19	
22	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	'694 patent: Fig. 5: N+ layer (40c) under N epi layer (40)
23	first portion, said second portion being lighter doped than said first portion.	
24	CLAIM 20	
25	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	'694 Patent and '297 Patent: avalanche breakdown would be a reach-through breakdown across the N epi
26	second portion.	layer
26	CLAIM 22	'297 Patent: oxide (14)
27	21. The method of claim 17 further comprising the step of providing an insulator between said surface of said	257 Fatcht. Oxide (14)
28	trench and said gate.	

1	CLAIM 23	·
_	23. A method for providing a transistor, said method	'694 Patent: Integrated Bipolar-MOS Semiconductor
2	comprising the steps of:	Device with Common Collector and Drain
3		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
4	providing a first region of a first conductivity type;	
5	providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	'694 Patent: Fig. 2: N-Epi layer (40) '297 Patent: Figs. 4-6: N layer (10)
6	providing a third region of a second conductivity type	'694 Patent: Fig. 2: P layer (42), (42a) and (42e)
	over said second region, said second and third regions	05/11 a.c. 1.g. 2.1 a.g. (12), (12),
7	forming a junction;	'297 Patent: Figs. 4-6: P layer (12)
8	providing a fourth region of said first conductivity type over said third region;	'694 Patent: Fig. 2: N+ layer (44) partly lying over P layer (42a) and (42e)
9		'297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
10	providing a trench through said fourth region and third regions; and	'297 Patent: Figs. 4-6: trench (18) through N layer (16) and P layer (12)
11	providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
12	wherein a deepest part of said third regions is laterally spaced from said trench;	'694 Patent: Fig. 5: the deepest part of the P region (42e) is laterally spaced form said trench
13	wherein a distance between said deepest part of said third region and said first region is less than a depletion	'694 and '297: a distance between said deepest part of a third region and a first region would be less than a
14	width of a planar junction which has the same doping profile as does said junction between said second and	depletion width of a planar junction which has the same doping profile as does said junction between a second
15	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
16	CLAIM 24	
17	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said	'694 Patent: Fig. 5: a portion of the P layer is a heavily doped P+ region (42e) and extends both vertically
18	third region which part is adjacent said trench.	upward and downward; P+ region (42e) is more heavily doped than P region (42a) which is near the gate region.
19		

20	INVALIDITY CLAIM CHART	FOR U.S. PATENT NO. 5,072,266
21	U.S. Patent 5,072,266	U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297
22	CLAIM 1	
23	1. A trench DMOS transistor cell comprising:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier
24		Density Beneath the Gate Oxide
25		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
26	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer
27	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'302 Patent: Figs. 20 and 22: N layer (100)
••	, , , , , , , , , , , , , , , , , , , ,	'297 Patent: Figs. 4-6: N layer (10)

DOCSSV2:500277.1

RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

1	a second covering layer of semiconductor material of	'302 Patent: Figs. 20 and 22: P layer (220) and (221)
	second electrical conductivity type lying on the first	
2	covering layer;	'297 Patent: Figs. 4-6: P layer (12)
	a third covering layer of semiconductor material of	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171)
3	heavily doped said first electrical conductivity type and	partly lying over P layer (220) and (221) where a portion
:	having a top surface and partly lying over the second	of the P layer (220) and (221) is heavily doped P+ and
4	covering layer, wherein a portion of the second covering	extends vertically upward through the N+ layer (170) and
ļ	layer is heavily doped and this portion extends both	(171) and vertically downward into the N layer (100)
5	vertically upward and downward, an upward portion	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
_	extending through the third covering layer to the top	layer (12)
6	surface of the third covering layer and a downward	\
_ :	portion extending downward into the first covering	
7	layer;	(207 P-+
	a trench having a bottom surface and side surfaces and	'297 Patent: Figs 4-6: trench (18) extends downward from the top surface of the N layer (16) through the N
8	extending vertically downward from the top surface of	layer (16), P layer (12) and through a portion of the N
9	the third covering layer through the third covering layer	layer (10)
9	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	
10	the trench lies above a lowest part of the downward	
10	portion of the second covering layer;	
11	electrically conducting semiconductor material	'297 Patent: conductive semiconductor material (24)
••	positioned within the trench;	257 2 200 200 200 200 200 200 200 200 200
12	a layer of oxide positioned within the trench between the	'297 Patent: oxide (14)
	electrically conducting semiconductor material and the	
13	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	'320 Patent: gate (132), source (210) and drain (270)
14	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	'297 Patent: electrodes coupled to the gate (24), source
15		(22) and drain (20)

16		·
17	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
18	U.S. Patent No. 5,298,442	U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297
19	CLAIM 17	
20	17. A method for providing a transistor, said method comprising the steps of:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide
21		'297 Patent: MOS Field-Effect Transistor with a One-
22	-	Micron Vertical Channel
23	providing a first region of a first conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer and N layer (100)
		'297 Patent: Figs. 4-6: N layer (10)
24	providing a second region of a second conductivity type over said first region;	'302 Patent: Figs. 20 and 22: P+ layer (220) and (221) lying over the N layer (100)
25	•	'297 Patent: Figs. 4-6: P layer (12)
26	providing a third region of said first conductivity type such that said first and third regions are separated by	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171) partly lying over P layer (220) and (221)
27	said second region;	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
28		layer (12)

1	providing a trench through said third and second regions; and	'297 Patent: Figs. 4-6: trench (18) through the N layer (16) and the P layer (12)
2	providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
_	wherein a portion P of said second region, which portion	'302 patent and '297 patent: the deep P+ region (220)
3	is spaced from said trench, extends deeper than said	and (221) of the '302 patent would be below the lowest
-	trench so that, if a predetermined voltage is applied to	point of the trench (18) of the '297 patent
4	said gate and to said third region and another	policies and the second control of the second
	predetermined voltage is applied to said first region, an	
5	avalanche breakdown occurs away from a surface of	
	said trench.	
6		
	•	
7	CLAIM 18	
	18. The method of claim 17 wherein said portion P of	'302 Patent: Figs. 20 and 22: a portion of the P layer is
8	said second region is doped heavier than another portion	heavily doped P+ region (220) and (221); the P+ region
9	of said second region which portion is adjacent said	(220) and (221) could be doped heavier than the P region
	trench.	adjacent the gate region.
10		
	CLAIM 19	
11		(202 motor): Fire 20 and 22, NJ, 11NJ, 1
	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	'302 patent: Figs. 20 and 22: N+ layer under N- layer (100)
12	first portion, said second portion being lighter doped	(100)
	than said first portion.	
13	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	'302 Patent and '297 Patent: avalanche breakdown
14	breakdown is a reach-through breakdown across said	would be a reach-through breakdown across the N- layer
	second portion.	(100)
15	CLAIM 22	
16	21. The method of claim 17 further comprising the step	'297 Patent: oxide (14)
10	of providing an insulator between said surface of said	` ` `
17	trench and said gate.	· .
•	CLAIM 23	T
18	23. A method for providing a transistor, said method	'302 Patent: Process for Manufacture of High Power
	comprising the steps of:	MOSFET with Laterally Distributed High Carrier
19		Density Beneath the Gate Oxide
		•
20		'297 Patent: MOS Field-Effect Transistor with a One-
ļ		Micron Vertical Channel
21	providing a first region of a first conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer
	providing a second region of said first conductivity type	'302 Patent: Figs. 20 and 22: N layer (100)
22	over said first region, said second region being lighter	'207 Patent: Figs. 4.6: N. Jayor (10)
_	doped than said first region;	'297 Patent: Figs. 4-6: N layer (10)
23	providing a third region of a second conductivity type	'302 Patent: Figs. 20 and 22: P layer (220) and (221)
, l	over said second region, said second and third regions forming a junction;	'297 Patent: Figs. 4-6: P layer (12)
24	providing a fourth region of said first conductivity type	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171)
25	over said third region;	partly lying over P layer (220) and (221)
ادع	over said unite togicit,	paray tying over 1 tayer (220) and (221)
26		'297 Patent: Figs. 4-6: N layer (16) partly lying over P
20		layer (12)
27	providing a trench through said fourth region and third	'297 Patent: Figs. 4-6: trench (18) through N layer (16)
-	regions; and	and P layer (12)
28	providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
	DOCSSV2:500277.1	RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b)
	,	(Case No. C-99-04797 SRA)

1	wherein a deepest part of said third regions is laterally spaced from said trench;	'302 Patent: Figs 20 and 22: deepest part the third (220) and (221) is laterally spaced from said gate region
2	wherein a distance between said deepest part of said	'302 and '297: a distance between said deepest part of a
	third region and said first region is less than a depletion	third region and a first region would be less than a
3	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
	profile as does said junction between said second and	doping profile as does said junction between a second
4	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
5		voltage.
	CLAIM 24	
6	24. The method of claim 23 wherein said deepest part of	'302 Patent: Figs. 20 and 22: a portion of the P layer is a
	said third region is doped heavier than a part of said	heavily doped P+ region (220) and (221) and extends
7	third region which part is adjacent said trench.	both vertically upward and downward; P+ region (220)
		and (221) could be more heavily doped than P region
8	~	which is near the gate region.
· 1		

Fairchild reserves the right to revise and supplement the claim analysis upon further discovery, investigation and analysis prior to the close of discovery. Additionally, the claim construction found by the Court may significantly alter Fairchild's invalidity arguments.

Fairchild asserts that the '266 and '442 patents are invalid under 35 U.S.C. § 112, ¶ 1, as not containing a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention.

Additionally, Fairchild asserts that claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent are invalid as being indefinite under the 35 U.S.C. § 112, ¶ 2. Claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent fail to distinctly claim the subject matter of the invention. For example, the limitation of claim 23 of the '442 patent "wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage" is indefinite under 35 U.S.C § 112, ¶ 2.

Additionally, Fairchild reserves the right to raise a best mode defense upon completion of discovery, specifically upon completion of the depositions of the inventors

ORRICK HERRINGTON

SUTCLIFFE LLP

		·	
1	In defense of Siliconix's allegation of willful infringement, Fairchild intends to rel		
2	upon the opinion(s) of counsel Townsend, Townsend & Crew dated December 23, 1998 and		
3	December 8, 1999. Supplemental invalidity/non-infringement opinion(s) will soon be provided to		
4	trial counsel.	• 	
5	Dated: August 30, 2000.	•	
6		TERRENCE P. MCMAHON	
7		WILLIAM L. ANTHONY, JR MONTE COOPER	
8		KAI TSENG THOMAS J. GRAY	
. 9		ORRICK, HERRINGTON & SUTCLIFFE LLP	
10		K. Jane	
11	·	Kai Tseng Attorneys for Defendant	
12		FAIRCHILD SEMICONDUCTOR, INC.	
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TERRENCE P. McMAHON (State Bar No. 71910) WILLIAM L. ANTHONY, JR. (State Bar No. 106908) MONTE COOPER (State Bar No. 196746) KAI TSENG (State Bar No. 193756) THOMAS J. GRAY (State Bar No. 191411) ORRICK, HERRINGTON & SUTCLIFFE LLP 1020 Marsh Road Menlo Park, CA 94025 Telephone: (650) 614-7400 Facsimile: (650) 614-7401 Attorneys for Defendant,

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SILICONIX INCORPORATED, a Delaware corporation

FAIRCHILD SEMICONDUCTOR

Plaintiff.

FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,

Defendant.

CASE NO: C99-04797 SBA

AMENDED INITIAL DISCLOSURE OF DEFENDANT FAIRCHILD SEMICONDUTOR - PRIOR ART PURSUANT TO CIVIL LOCAL RULE 16-7

AMENDED INITIAL DISCLOSURE OF PRIOR ART PURSUANT I. TO L.R. 16-7(D)

Pursuant to Local Rule 16-7(d), defendant Fairchild Semiconductor Corporation ("Fairchild") makes the following amended initial disclosure of prior art:

Attached hereto is Fairchild's amended initial disclosure of prior art patents, products and publications, and tables categorizing those references. Fairchild's investigation, and its analysis of the listed references, is continuing, and Fairchild reserves the right to supplement and to revise the information provided herein as further analysis is performed, additional information becomes available and discovery is completed. All patents are U.S. patents unless otherwise noted. On information and belief, each listed publication was published at least as early as the date given.

10414-4 JG3

DOCSSV2:503110.1

AMENDED INITIAL DISCLOSURE OF PRIOR ART C 99-04797 SBA

ORRICK, HERRINGTON & SUTCLIFFE LLP

Fairchild incorporates, in full, all references cited (however partially) in the patents-in-suit and/or in their respective file histories, as if fully set forth herein. 2 3 While Fairchild will preliminarily identify pursuant to Local Rule 16-7(e) the prior art references which Fairchild believes anticipates the asserted claims or the combination of 4 prior art references which render the asserted claims obvious, please note that the information in 5 this document is provisional and subject to revision, for the following reasons: 6 7 Fairchild's position on the invalidity of particular claims will depend on (i) how those claims are construed by the Court. Because claim construction has not yet occurred, 8 Fairchild cannot take a final position on the bases for invalidity of disputed claims because the 9 Court may construe those claims to mean something different from what Fairchild presently 10 11 assumes them to mean. 12 Fairchild's search for prior art is on-going. (ii) 13 Fairchild has not completed its discovery from Siliconix Inc. Depositions (iii) 14 of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventors, 15 for instance, will likely reveal information that affects the conclusions herein. 16 PRODUCTION OF DOCUMENTS PURSUANT TO L.R. 16-7(F) II. 17 As required by Local Rule 16-7(f), Fairchild has already produced technical documentation for the Fairchild FDS6680A, the only product accused of infringement in 18 19 Siliconix's Claim Chart. 20 The undersigned certifies that pursuant to local rule 16-6(c) to the best of his knowledge information and belief, formed after a reasonable inquiry, that the disclosure is 21 22 complete and correct, as of this date. 23 Dated: August 30, 2000 24 ORRICK, HERRINGTON & SUTCLIFFE LLP 25 26 27 Attorneys for Defendant 28 Fairchild Semiconductor Corporation ORRICK, HERRINGTON DOCSSV2:503110.1 -2-& SUTCLIFFE LLP 10414-4 103 AMENDED INITIA. SCLOSURE OF PRIOR ART C 99-04797 SBA

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AMENDED INITIAL DISCLOSURE OF PRIOR ART U.S. Patents No. 5,072,266 & 5,298,422

SILICONIX INC. VS. FAIRCHILD SEMICONDUCTOR CORPORATION

		ACCIONEDIO E	ZEMETE	PIEL CATION	
		INVENTOR		DATE	
-	Mos Field-Effect Transistor	P.R. Amlinger	U.S. PT. NO.	11/19/68	103
	With A One-Micron Vertical	•	3,412,297		
	Channel				
2	Integrated Circuit Utilizing	Jean-Claude Frouin et	U.S. PT. NO.	03/10/70	103
	Dielectric Plus Junction	al.	3,500,139		
	Isolation				
w	Complementary Field-Effect	Roger Cullis	U.S. PT. NO.	06/30/70	103
	Transistors On Common		3,518,509		
	Substrate By Multiple Epitaxy				
	Techniques				
4	Modified Planar Process For	Loyd H. Clevenger	U.S. PT. NO.	10/13/70	
	Making Semiconductor		3,534,234		
	Devices Having Ultrafine		,		
	Mesa Type Geometry				
5	Method Of Fabricating	Peltzer	U.S. PT. NO.	03/07/72	103
	Integrated Circuits, With		3,648,125		
	Integrated Circuits With				
	Oxidized Isolations And The				
-	Resulting Structure				

NO.	PATENT OR	AUTHOR/	PATENT	ISSUE/	CLASSIFICATION
	PUBLICATION THEE	INVENTOR	NONDEX	DATE	
6	Method Of Manufacturing	Appels et al.	U.S. PT. NO.	08/19/75	103
	Semiconductor Devices In		3,900,350		
	Which Silicon Oxide Regions				
	Inset In Silicon Are Formed				
	By A Masking Oxidation,				
	Wherein An Intermediate				
	Layer Of Polycrystalline				
	Silicon Is Provided Between			•	
	The Substrate And The	-			
	Oxidation Mask				
7	Low Capacitance V. Grove	Rodgers	U.S. PT. NO.	12/02/75	102, 103
	Mos Nor Gate And Method		3,924,265		
	Of Manufacture				
œ	Multilevel Conductor	Naber	U.S. PT. NO.	12/09/75	103
	Structure And Method		3,925,572		
y	Semiconductor Device	Webb	U.S. PT. NO.	05/18/76	
	Manufacture		3,958,040		
10	Semiconductor Device	Abbas et al.	U.S. PT. NO.	06/01/76	
	Having Electrically Insulating	-	3,961,355		
-	Barriers For Surface Leakage				
	Sensitive Devices And				
	Method Of Forming				
=	Method For Forming	Antipov	U.S. PT. NO.	06/08/76	
	Recessed Dielectric Isolation		3,961,999		
	With A Minimized "Birds				
	Beak" Problem				

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, —	20	3	10	8				17				16			15				14		<u></u>					12			NC.
	Large Value Capacitor	Device Scilledidución	Field Effect Semiconductor	Single Igfet Memory Cell With Buried Storage Flement	Produced Thereby	And Novel Mask Structures	Comprising Silicon Nitride	Method For Forming Musks	Polycrystalline Growth	Utilizing Monocrystalline-	Semiconductor Device	Method Of Manufacturing A	Semiconductor Device	Electrical Contacts On A	Method Of Forming Raised	Produced By Said Method	Semiconductor Device	Semiconductor Device And A	Method For Producing A	Semiconductor Devices	Dielectrically Isolated	Oxidation	Deposition And Thermal	Combining Dielectric	Dielectric Isolation	Method For Forming		PUBLICATION TITLE	PATENT OR
	Kendall et al.	ב מאמנם	Knkura	Jenne				Magdo et al.				Kaji et al.		·	Reichert			•	Kooi		Hochberg					Feng et al.	INVENTOR	ASSIGNEE/OR	AUTHOR
4,017,885	U.S. PT. NO.	4,015,278	11 & DT NO	U.S. PT. NO. 4 003 036			4,002,511	U.S. PT. NO.			3,977,378	U.S. PT. NO.		3,993,515	U.S. PT. NO.			3,970,486	U.S. PT. NO.	3,966,577	U.S. PT. NO.				3,966,514	U.S. PT. NO.		NUMBER	PATENT
	04/12/77	03123111	03/20/77	01/11/77				01/11/77				12/14/76			11/23/76				07/20/76		06/29/76					06/29/76	DATE	PUBLICATION	ISSUE/
,				103																					•				CLASSIFICATION

	09/19/78	U.S. PT. NO.	Masuoka et al.	Semiconductor Memory	30
103	08/08/78	U.S. PT. NO. 4,105,475	Jenne	Epitaxial Method Of Fabricating Single Igfet Memory Cell With Buried Storage Element	29
103	08/01/78	U.S. PT. NO. 4,104,086	Bondur et al.	Method For Forming Isolated Regions Of Silicon Utilizing Reactive Ion Etching	28
	07/18/78	U.S. PT. NO. 4,101,922	Tihani et al.	Field Effect Transistor With A Short Channel Length	27
103	02/07/78	U.S. PT. NO. 4,072,975	Ishitani	Insulated Gate Field Effect Transistor	26
103	01/24/78	U.S. Pt. No. 4,070,690	Wickstrom	Vmos Transistor	25
103	12/27/77	U.S. PT. NO. 4,065,783	Ouyang	Self-Aligned Double Implanted Short Channel V- Grove Mos Device	24
	11/01/77	U.S. PT. NO. 4,055,884	Jambotkar	Fabrication Of Power Field Effect Transistors And The Resulting Structures	23
103	09/13/77	U.S. PT. NO. 4,048,649	Bohn .	Superintegrated V-Grove Isolated Bipolar And Vmos Transistors	22
	09/06/77	U.S. PT. NO. 4,046,605	Nelson et al.	Method Of Electrically Isolating Individual Semiconductor Circuits In A Wafer	21
CLASSIFICATION	ISSUE/ PUBLICATION DATE	PATENT NUMBER	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT OR PUBLICATION TITLE	NO.

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103	04/22/80	US PT NO	Natori et al	Semiconductor Memory	95
- 123	04/15/80	U.S. PT. NO. 4,198,693	Kuo	VMOS Read Only Memory	86
				Semiconductor Devices	
	10/03/13	4,170492		Oxidation In Manufacture Of	٥/
	05/00/01	4,104,731	Darker of all	Matha Official	3
	08/14/79	U.S. PT. NO.	Tasch, Jr.	High Capacity Dynamic Ram	
103					36
				Implantation	
				Structures Utilizing Ion-	
		4,159,915		Vertical NPN And PNP	
	07/03/79	U.S. PT. NO.	Anantha et al.	Method For Fabrication	35
		4,148,047		•	
103	04/03/79	U.S. PT. NO.	Hendrickson	Semiconductor Apparatus	34
		4,145,700		fransistors	
	03/20/79	U.S. PT. NO.	Jambotkar	Power Field Effect	33
				Etching And Diffusion	
******		4,140,558		Circuits Utilizing Selective	
103	02/20/79	U.S. PT. NO.	Murphy et al.	Isolation Of Integrated	32
				Capacitance	
				Dynamic Memory Cell	
		4,116,720		Field Effect Transistor For A	
103	09/26/78	U.S. PT. NO.	Vinson	Method Of Making V-MOS	15
	DATE		INVENTOR		
	PUBLICATIO	NOMBER	ASSIGNEE/OR	PUBLICATION TITLE	7.
CLASSIFICATION	ISSUE/	PATENT	AUTHOR/	PATENT OR	2

NC.	PATENT OR	AUTHOR/	PATENT	ISSUE/	CLASSIFICATION
	PUBLICATION TITLE	ASSIGNEE/OR INVENTOR	NUMBER	PUBLICATION DATE	
949	One Device Field Effect	Scheuerlein	U.S. PT. NO.	03/09/82	
,	Transistor (FET) AC Stable		4,319,342		
	Random Access Memory				
	(Ram) Array				
00	Method Of Fabricating MOS	Chang et al.	U.S. PT. NO.	04/13/82	
	Field Effect Transistors		4,324,038		
15	Method Of Manufacturing	lwai et al.	U.S. PT. NO.	05/04/82	
	Semiconductor Devices		4,327,476		
52	Insulated Gate Type	Nishizawa	U.S. PT. NO.	06/08/82	
	Semiconductor Device		4,334,235		
53	Combined DMOS And A	Pao et al.	U.S. PT. NO.	08/10/82	
•	Vertical Bipolar Transistor		4,344,081		
	Device And Fabrication				
	Method Therefor				
54	MOS Power Transistor With	Blanchard	U.S. PT. NO.	08/17/82	103
	Improved High-Voltage	-	4,345,265		
	Capability				
SS	Silicon Integrated Circuits	Jaccodine et al.	U.S. PT. NO.	10/05/82	
			4,353,086		
56	Power MOSFET With An	Becke et al.	U.S. PT. NO.	12/14/82	103
	Anode Region		4,364,073		
57	V-MOS Device With Self-	Garnache et al.	U.S. PT. NO.	12/14/82	102
	Aligned Multiple Electrodes		4,364,074		
S8	Semiconductor Integrated	Crowder et al.	U.S. PT. NO.	12/21/82	103
	Circuit Interconnections		4,364,166		
59	Vertical MOSFET With	Goodman et al.	U.S. PT. NO.	12/28/82	103
	Reduced Turn-On Resistance		4,366,495		
60	VMOS Memory Cell And	Hiltpold	U.S. PT. NO.	12/25/83	103
	Method For Making Same		4,369,564		

61 Method For Manufacturing A Coodman	NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR	PATENT NUMBER	ISSUE/ PUBLICATION	2
Vertical, Grooved MOSFET Power Static Induction Transistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.	61	Method For Manufacturing A	Goodman	U.S. PT. NO.	02/22/83	2/83
Power Static Induction Transistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysificon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Vertical, Grooved MOSFET		4,374,455		
Transistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	62	Power Static Induction	Cogan	U.S. PT. NO.	03/01/83	1/83
High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysificon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Matsumura et al. Matsumura et al.	•	Transistor Fabrication		4,375,124		
Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysiticon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Matsumura et al. Matsumura et al.	63	High Power MOSFET With	Lidow et al.	U.S. PT. NO.	03/0	03/08/83
Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process FET Memory Cell Structure Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Low On-Resistance And High		4,376,286		
Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Breakdown Voltage			·	
Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysificon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.	64	Method Of Fabricating A	Baliga et al.	U.S. PT. NO.	Ç	04/24/84
A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Semiconductor Device With		4,443,931		
Deep Portion Reactive Sputter Etching Of Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Maydan et al. Fatula Jr. et al. Fatula Jr. et al. Fatula Jr. et al. Makurai Fatula Jr. et al. Fatula Jr. et al. Makurai Matsumura et al. Matsumura et al.		A Base Region Having A				
Reactive Sputter Etching Of Polysiticon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Maydan et al. Maydan et al. Maydan et al. Maydan et al. Matsumura et al. Matsumura et al. Matsumura et al.		Deep Portion			1-	
Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.	8	Polysilicon Utilizing A	Maydan et al.	4.383.885		05/1 //83
FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Chlorine Etch Gas				
And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	99	FET Memory Cell Structure	Fatula Jr. et al.	U.S. PT. NO.		08/09/83
Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		And Process		4,397,075		
Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	67	Fabrication Method For High	Blanchard et al.	U.S. PT. NO.		08/16/83
Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Power MOS Device		4,398,339		
Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	89	Method For Manufacturing A	Sakurai	U.S. PT. NO.		09/20/83
A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Field Isolation Structure For		4,404,735		
Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		A Semiconductor Device				
Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	69	Planar Structure For High	Herman et al.	U.S. PT. NO.		10/25/83
Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Voltage Semiconductor		4,412,242		
Layer Over High Field Regions Semiconductor Device Matsumura et al.		Devices With Gaps In Glassy				
Regions Semiconductor Device Matsumura et al.		Layer Over High Field				
Semiconductor Device Matsumura et al.		Regions			-	
	70	Semiconductor Device	Matsumura et al.	U.S. PT. NO. 4,412,237	-	10/25/83

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Ç	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR	PATENT NUMBER	ISSUE/ PUBLICATION	CLASSIFICATION
71	Method Of Fabricating Mesa MOSFET Using Overhang Mask	Rice	U.S. PT. NO. 4,419,811	12/13/83	
72	Semiconductor Memory Device	Takei	U.S. PT. NO.	02/14/84	103
73	Enhancement Mode JFET	Nishizawa	4,432,006		
	Dynamic Memory	MSHZAWA	U.S. PT. NO.	02/28/84	
74	Fabrication of MOS	Fuls et al.	TIS DT NO	05500	
35	Integrated Circuit Devices		4,450,620	05/29/84	
2	Integrated Circuits	Joy et al.	U.S. PT. NO.	06/19/84	-
76	Isolation For High Density Integrated Circuits	Joy et al.	U.S. PT. NO.	06/19/84	
77			1,40,404/		
	Method Of Manufacturing A Self-Aligned U-MOS	lwai	U.S. PT. NO.	06/26/84	103
	Semiconductor Device		4,400,740		
78	Vertical MESFET With Guardring	Rice	U.S. PT. NO.	07/10/84	
79	Method For Manufacturing	Schwabe et al.	U.S. PT. NO.	07/17/04	
	VLSI Complementary MOS Field Effect Transistor		4,459,740	0//1//84	103
	Circuits In Silicon Gate				-
80	Single Electrode U-MOSFFT	Fig. et al.			
*	ļ		4,462,040	07/24/84	103
,	Insulated-Gate Semiconductor	Temple	U.S. PT. NO.	08/21/84	
	Devices With Integral Shorts		4,466,176		

Method For Mann Semiconductor D. Method Of Fabric Bipolar Dynamic Cell V-MOS Filed Ef. Transistor Method Of Fabric Method Of Fabric MoSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabri Isolation Region I Semiconductor D. Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D. Deep Grip Access The Surface And Method For Form Free Isolation Structuring S. Method For Form Free Isolation Structuring S. MoSFET With P. Channel	PATENT OR	AUTHOR	PATENT	ISSUE/
Method For Mann Semiconductor D. Method Of Fabric Bipolar Dynamic Cell V-MOS Filed Ef. Transistor Method Of Fabric Method Of Fabric Method Of Fabric Self-Aligned Diff Etching Techniqu Method For Fabril Isolation Region I Semiconductor D. Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D. Semiconductor D. Semiconductor D. Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D. Deep Grip Access The Surface And Manufacturing S. Method For Form Free Isolation Str. Utilizing Etch An Techniques MOSFET With P. Channel	PUBLICATION TITLE	ASSIGNEE/OR INVENTOR	NUMBER	PUBLICATION DATE
Semiconductor D. Method Of Fabric Bipolar Dynamic Cell V-MOS Filed Ef Transistor Method Of Fabric Method Of Fabric MoSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabril Isolation Region I Semiconductor D Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Stru Utilizing Etch An Techniques MOSFET With P Channel	Method For Manufacturing	Kameyama	U.S. PT. NO.	09/18/84
Method Of Fabric Bipolar Dynamic Cell V-MOS Filed Ef Transistor Method Of Fabric MoSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabri Isolation Region I Semiconductor D Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Stru Utilizing Etch An Techniques MOSFET With P Channel	Semiconductor Device	·	4,472,240	
Bipolar Dynamic Cell V-MOS Filed Ef Transistor Method Of Fabric MOSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabri Isolation Region I Semiconductor D Self-Aligned Pow With Integral Sou Short And Metho Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Stru Utilizing Etch An Techniques MOSFET With P Channel	Method Of Fabricating A	El-Karach	U.S. PT. NO.	10/16/84
Transistor Method Of Fabric Method Of Fabric MOSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabri Isolation Region I Semiconductor D Self-Aligned Pow With Integral Sou Short And Method Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Structuring Etch An Techniques MOSFET With P Channel	Bipolar Dynamic Memory Cell		4,476,623	
Transistor Method Of Fabric MOSFET Structu Self-Aligned Diff Etching Techniqu Method For Fabri Isolation Region I Semiconductor D Self-Aligned Pow With Integral Sou Short And Metho Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Stru Utilizing Etch An Techniques MOSFET With P Channel	V-MOS Filed Effect	David et al.	U.S. PT. NO.	03/05/85
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Semiconductor D. Self-Aligned Pow With Integral Sou Short And Metho Making Semiconductor D. Deep Grip Access The Surface And Manufacturing S. Method For Form Free Isolation Strr Utilizing Etch An Techniques MOSFET With P. Channel	Isolation Region In			04/09/60
Self-Aligned Pow With Integral Sou Short And Metho Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Strr Utilizing Etch An Techniques MOSFET With P Channel	Semiconductor Devices		4,509,249	04/02/83
With Integral Sou Short And Metho Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Stra Utilizing Etch An Techniques MOSFET With P Channel	Self-Aligned Power MOSFET		4,509,249	04/07/65
Short And Metho Making Semiconductor D Deep Grip Access The Surface And Manufacturing S. Method For Form Free Isolation Strr Utilizing Etch An Techniques MOSFET With P Channel	With Integral Source-Base	Love	4,509,249 U.S. PT. NO.	05/07/85
Making Semiconductor D Deep Grip Access The Surface And Manufacturing S Method For Form Free Isolation Strr Utilizing Etch An Techniques MOSFET With P Channel	Short And Methods Of	Love	4,509,249 U.S. PT. NO. 4,516,143	05/07/85
Semiconductor D. Deep Grip Access The Surface And Manufacturing S. Method For Form Free Isolation Str Utilizing Etch An Techniques MOSFET With P Channel	Aaking	Love	4,509,249 U.S. PT. NO. 4,516,143	05/07/85
Deep Grip Access The Surface And Manufacturing S. Method For Form Free Isolation Str Utilizing Etch An Techniques MOSFET With P Channel		Love	4,509,249 U.S. PT. NO. 4,516,143	05/07/85
The Surface And Manufacturing S. Method For Form Free Isolation Stri Utilizing Etch An Techniques MOSFET With P Channel	Semiconductor Device With	Love Arnould et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO.	05/07/85
Manufacturing S. Method For Form Free Isolation Str Utilizing Etch An Techniques MOSFET With P Channel	Semiconductor Device With Deep Grip Accessible Via	Love Arnould et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552	05/07/85
Method For Form Free Isolation Str Utilizing Etch An Techniques MOSFET With P Channel	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For	Love Arnould et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552	05/07/85
Free Isolation Structure Utilizing Etch An Techniques MOSFET With P	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same	Love Arnould et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552	05/07/85
Utilizing Etch An Techniques MOSFET With P	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void	Love Arnould et al. Beyer et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO.	05/07/85
Techniques MOSFET With P Channel	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void Free Isolation Structure	Love Arnould et al. Beyer et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047	05/07/85
MOSFET With P Channel	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void Free Isolation Structure Utilizing Etch And Refill	Love Amould et al. Beyer et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047	05/07/85
Channel	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void Free Isolation Structure Utilizing Etch And Refill Techniques	Love Arnould et al. Beyer et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047	05/07/85
	he Surface And Process For Manufacturing Same Method For Forming A Void ree Isolation Structure Julizing Etch And Refill echniques	Love Arnould et al. Beyer et al. Ford et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047 U.S. PT. NO.	05/07/85
One Transistor D	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void Free Isolation Structure Utilizing Etch And Refill Techniques MOSFET With Perimeter Channel	Love Amould et al. Beyer et al. Ford et al.	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047 U.S. PT. NO. 4,532,534	05/07/85 06/04/85 07/09/85
Random Access Memory	Semiconductor Device With Deep Grip Accessible Via The Surface And Process For Manufacturing Same Method For Forming A Void Free Isolation Structure Utilizing Etch And Refill Techniques MOSFET With Perimeter Channel One Transistor Dynamic	Love Armould et al. Beyer et al. Ford et al. Gibbons	4,509,249 U.S. PT. NO. 4,516,143 U.S. PT. NO. 4,520,552 U.S. PT. NO. 4,528,047 U.S. PT. NO. 4,532,534 U.S. PT. NO.	05/07/85 06/04/85 07/09/85 07/30/85

Publicational Power With Schutten et al. U.S. PT. NO. 10/08/85 103	NO.	PATENT OR	AUTHOR/	PATENT	ISSUE/	CLASSIFICATION
Bidirectional Power With Substrate-Referenced Shield Lateral Bidirectional Notch FET With Extended Gate Insulator Bidirectional Power FET Bidirectional Power FET Bidirectional Power FET Schutten et al. With Field Shaping Schutten et al. U.S. PT. NO. 10/08/85 FIEL With Extended Gate Insulator Bidirectional Power FET Bidirectional Power FET Schutten et al. U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/12/85 Duplicate U.S. PT. NO. 11/12/85 Levinstein et al. U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/12/85 Levinstein et al. U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/12/85 Levinstein et al. U.S. PT. NO. 11/12/85 U.S. PT. NO. 02/03/86 Integrated Semiconductor Circuit Devices Manufacturing U.S. PT. NO. 02/03/86 U.S. PT. NO. 04/15/86		PUBLICATION TITLE	ASSIGNEE/OR INVENTOR	NUMBER	PUBLICATION DATE	
Substrate-Referenced Shield Lateral Bidirectional Notch FET With Extended Gate Insulator Bidirectional Power FET Bidirectional Power FET Schutten et al. With Field Shaping Duplicate Simplified Planarization Filted Trenches Method Of Fabricating VLSI Complementary Threshold Voltages Inversion-Mode Insulated-Gate Gate Chamiel Field Controlled Device Employing A Recessed Gate Structure Method Of Manufacturing of Lidow, et al. High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Shepard U.S. PT. NO. 11/12/85 U.S. PT. NO. 11/26/85 U.S. PT. NO. 11/26/85 U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86	92	Bidirectional Power With	Schutten et al.	U.S. PT. NO.	09/10/85	103
Lateral Bidirectional Notch FET With Extended Gate Insulator Bidirectional Power FET Bidirectional Power FET With Field Shaping With Field Shaping Duplicate Simplified Planarization Process For Polysilicon Filled Trenches Method Of Fabricating VLSI Complementary Threshold Voltages Inversion-Mode Insulated-Gate Galtium Arsenide Field-Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing of Lidow, et al. High Power MOSEFT with Laterally Distributed High Carrier Density Beneath The Cate Oxide U.S. PT. NO. 11/26/85 LUS. PT. NO. 11/26/85 U.S. PT. NO. 12/3/85 U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86		Substrate-Referenced Shield		4,541,001		
HET With Extended Gate Insulator Bidirectional Power FET Bidirectional Power FET With Field Shaping Duplicate Simplified Planarization Process For Polysiticon Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated-Gate Galtium Arsenide Field-Gate Galtium Arsenide Field-Baliga et al. Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing of Circuit Devices High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide A,545,728 LIVI2/85 Levinstein et al. U.S. PT. NO. 11/26/85 Levinstein et al. U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86	93	Lateral Bidirectional Notch	Schutten et al.	U.S. PT. NO.	10/08/85	103
Bidirectional Power FET With Field Shaping Duplicate Simplified Planarization Process For Polysilicon Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing of Lidow, et al. Process for Manufacturing of Lidow, et al. Laterally Distributed High Cartier Density Beneath The Gate Oxide U.S. PT. NO. 11/26/85 U.S. PT. NO. 02/03/86	•	FET With Extended Gate		4,546,367		
Bidirectional Power FET With Field Shaping Duplicate Simplified Planarization Process For Polysilicon Filled Trenches Method Of Fabricating VLSI Complementary Threshold Voltages Inversion-Mode Insulated- Gate Galtum Arsenide Field- Effect Transistors Method Of Making Vertical Device Employing A Recessed Gate Structure Method of Manufacturing of Circuit Devices Process for Manufacturing of Lidow, et al. Laterally Distributed High Carrier Density Beneath The Gate Oxide Duplicate U.S. PT. NO. 11/26/85 U.S. PT. NO. 12/3/85 U.S. PT. NO. 12/3/85 U.S. PT. NO. 12/3/86 U.S. PT. NO. 14/5/86 U.S. PT. NO. 14/5/86		Insulator				
Mith Field Shaping Simplified Planarization Process For Polysilicon Filled Trenches Filled Controlled	94	Bidirectional Power FET	Schutten et al.	U.S. PT. NO.	11/12/85	
Simplified Planarization Process For Polysilicon Filled Trenches Filled Trenches Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Callium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing Integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Device Simplified Planarization Shepard 4,554,728 Levinstein et al. U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86		With Field Shaping		4,553,151		
Simplified Planarization Process For Polysilicon Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Callium Arsenide Field- Effect Transistors Method Of Making Vertical Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of Lidow, et al. High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Shepard 4,554,728 U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86	95		Duplicate			
Process For Polysilicon Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing Integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide 4,554,728 U.S. PT. NO. 12/3/85 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86	96	Simplified Planarization	Shepard	U.S. PT. NO.	11/26/85	
Filled Trenches Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing Integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Method Of State Structure Lidow, et al. U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86		Process For Polysilicon		4,554,728		
Method Of Fabricating VLSI CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Device Employing A Recessed Gate Structure Method of Manufacturing of Circuit Devices High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Method Of Fabricating VLSI 4,555,842 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86		Filled Trenches				
CMOS Devices Having Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide 4,555,842 U.S. PT. NO. 02/03/86 U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86	97	Method Of Fabricating VLSI	Levinstein et al.	U.S. PT. NO.	12/3/85	
Complementary Threshold Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Complementary Threshold Baliga U.S. PT. NO. U.S. PT. NO. 4,571,815 U.S. PT. NO. 4,582,565 U.S. PT. NO. 4,582,565 U.S. PT. NO. 4,582,565 U.S. PT. NO. 4,582,362		CMOS Devices Having		4,555,842		
Voltages Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing Integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide U.S. PT. NO. 02/03/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86		Complementary Threshold				
Inversion-Mode Insulated- Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86		Voltages	•			
Gate Gallium Arsenide Field- Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide 4,588,958 U.S. PT. NO. 02/25/86 4,571,815 U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86 4,593,302	98	Inversion-Mode Insulated-	Baliga	U.S. PT. NO.	02/03/86	103
Effect Transistors Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Carrier Density Beneath The Gate Oxide U.S. PT. NO. 02/25/86 U.S. PT. NO. 04/15/86 U.S. PT. NO. 04/15/86 4,582,565 U.S. PT. NO. 06/03/86		Gate Gallium Arsenide Field-		4,568,958		
Method Of Making Vertical Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Carrier Density Beneath The Gate Oxide Method Of Making Vertical Baliga et al. 4,571,815 U.S. PT. NO. 4,582,565 U.S. PT. NO. 4,593,302 U.S. PT. NO. 4,593,302		Effect Transistors				
Channel Field Controlled Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide 4,571,815 U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86	99	Method Of Making Vertical	Baliga et al.	U.S. PT. NO:	02/25/86	
Device Employing A Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Device Employing A U.S. PT. NO. 4,582,565 U.S. PT. NO. 06/03/86 4,593,302		Channel Field Controlled		4,571,815		
Recessed Gate Structure Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Rawakatsu U.S. PT. NO. 04/15/86 U.S. PT. NO. 06/03/86 4,593,302		Device Employing A				
Method of Manufacturing integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Manufacturing of Lidow, et al. Lidow, et al. U.S. PT. NO. 4,593,302 4,593,302		Recessed Gate Structure				
integrated Semiconductor Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide 4,582,565 U.S. PT. NO. 06/03/86 4,593,302	100	Method of Manufacturing	Kawakatsu	U.S. PT. NO.	04/15/86	
Circuit Devices Process for Manufacturing of High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide Circuit Devices U.S. PT. NO. 06/03/86 4,593,302		integrated Semiconductor		4,582,565		
Process for Manufacturing of Lidow, et al. U.S. PT. NO. 06/03/86 High Power MOSFET with Laterally Distributed High Carrier Density Beneath The Gate Oxide		Circuit Devices				
4,593,302	101	Process for Manufacturing of	Lidow, et al.	U.S. PT. NO.	06/03/86	103
Carrier Density Beneath The Gate Oxide		High Power MOSFET with		4,593,302		
Carrier Density Beneath The Gate Oxide		Laterally Distributed High				
Gate Oxide		Carrier Density Beneath The				
		Gate Oxide				

				sidewalls of isolation trenches	
	02/03/87	H204	Oh et al.	Method for implanting the	116
				polycrystalline silicone	
				silicides having a high	
				double layers of metal	•
		4,640,844		of gate electrodes formed of	
	02/03/97	U.S. PAT NO.	Neppl et al.	Method for the manufacture	109
		4,639,754		Diminished Bipolar Effects	
103	01/27/87	U.S. PT. NO	Wheatley, Jr. et al.	Vertical MOSFET with	801
				An Insulating Trench	
				Field Oxide With Respect To	•
		4,636,281		Autopositioning Of A Local	
	01/13/87	U.S. PT. NO	Buiguez et al.	Process For The	107
		4,631,803		Free Trench Isolation Devices	
	12/20/86	U.S. PT. NO	Hunter et al.	Method of Fabrication Defect	106
103	12/16/86	U.S. PT. NO 4,630,088	Ogura et al.	MOS Dynamic Ram	105
				Terminal Means	
				Dual Gate Reference	
				Channel Stacking And With	
		4,622,569		FET With Notched Multi-	
103	11/11/86	U.S. PT. NO	Lade et al.	Lateral Bidirectional Power	104
		4,608,584		Transistor	
103	08/24/86	U.S. PT. NO	Mihara	Vertical Type MOS	103
				Its Manufacture	
		4,596,999		Component And Process For	
	06/24/86	U.S. PT. NO	Gobrecht et al.	Power Semiconductor	102
	DATE		INVENTOR		-
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20	PATENT OR	AUTHOR	PATENT	ISSUE/	CLASSIFICATION
Ś	PUBLICATION TITLE	ASSIGNEE/OR INVENTOR	NUMBER	PUBLICATION DATE	
Ξ	Dynamic memory device	Lu	U.S. PAT NO.	03/17/87	
	having a single-crystal		6,649,625		
	transistor on a trench				
	capacitor structure and a				
	fabrication method therefor				
112	Shallow grove capacitor	Erb et al.	U.S. PAT NO.	03/17/87	
	fabrication method		4,650,544		
113	Dynamic memory device	Lu	U.S. PAT NO.	03/17/87	
	having a single-crystal		4,649,625		
	transistor on a trench	•			
	capacitor structure and a				
	fabrication method therefor				
114、	Dram cell and array	Malhi	4.651 184 .	03/17/87	103
15	Complementary mos	Sunami et al.	U.S. PAT NO.	06/02/87	
	integrated circuits having		4,670,768		
	vertical channel fets				
116	Semiconductor memory	Miura et al.	U.S. PAT NO.	06/09/87	103
	device with trench		4,672,410		
	surrounding each memory cell				
117	Vertical dram cell and method	Chatterjee et al.	U.S. PAT NO. 4,673,962	06/16/87	103
811	mos transistor	Terry et al.	U.S. PAT NO. 4,675,713	06/23/87	103
119	Process for manufacture of	Lidow et al.	U.S. PAT NO.	07/21/87	103
	high power mosfet with		4,680,853		
	laterally distributed high				
	carrier density beneath the				
	gate oxide				

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Roger Cullis United Kingdom 09/27/67 1084937 France 11/07/69 2.003.068	129	High density memory with field shield	Kenney	U.S. PAT NO. 4,751,588	06/14/88	
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	Trenches with a Rounded				
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	Semiconductor Subtrate				
	having Insulating Sidewalls				
	and Bottom with Polysilicon,				
	Forming, Then Oxidizing the		•		
	Upper Surface of a				
	Polysilicon Layer Which				
	Extends over the Sidewalls		•	•	

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